

PXN7R1-30RLA

N-channel 30 V, 7.1 mOhm, logic level Trench MOSFET in MLPAK56

29 January 2026 **Product data sheet**

1. General description

General purpose MOSFET for standard applications, 55 A, logic level N-channel enhancement mode Power MOSFET in MLPAK56 package.

2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Small footprint (5 x 6 mm) for compact design

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Battery Management System
- Motor drive
- Load switching

4. Quick reference data

Table 1. Quick reference data

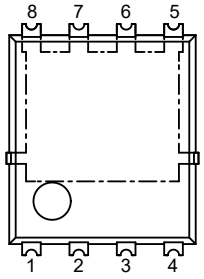
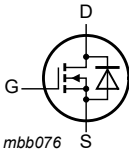
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	55	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	35	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	5.7	7.1	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	7.8	10.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 11; Fig. 12		-	1.1	-	nC
$Q_{G(tot)}$	total gate charge			-	5	-	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 18.2 A; V_{sup} ≤ 30 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	-	33.1	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V; T_j = 25 °C; Fig. 15	[2]	-	3.3	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK56-WF (SOT8038-2)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN7R1-30RLA	MLPAK56-WF	MLPAK56-WF: 8 terminals; body 5.15 x 6.2 x 1.0 mm	SOT8038-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN7R1-30RLA	N7R1-30

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

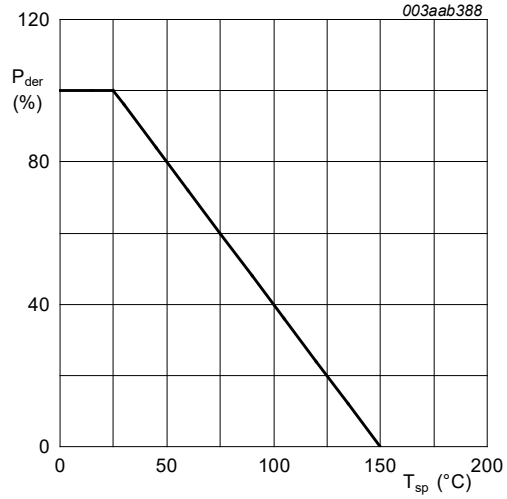
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	35	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	55	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	34	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	218	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	29	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	218	A

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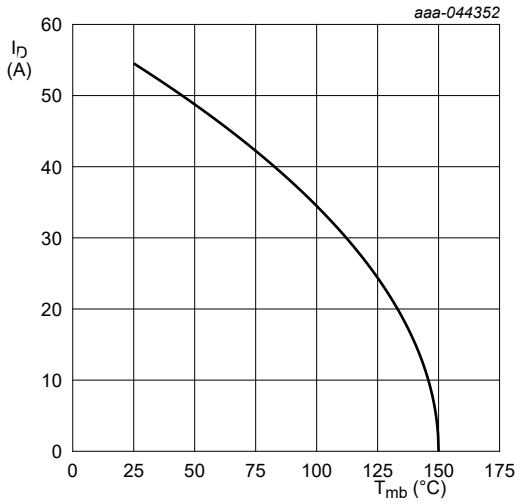
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 18.2 A; V_{sup} ≤ 30 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	33.1	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[1]	-	18.2	A

[1] Protected by 100% test



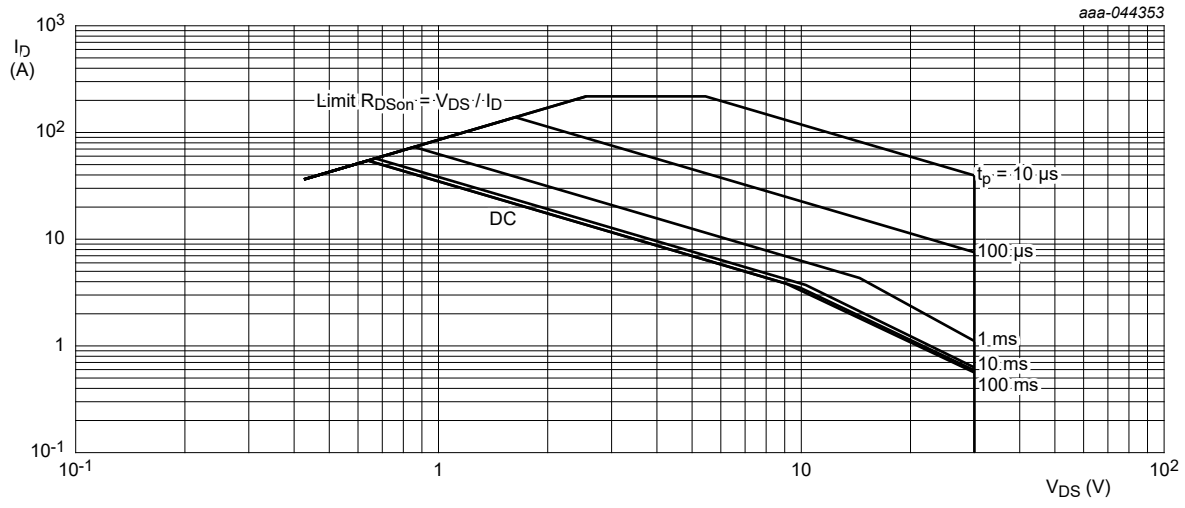
$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



VGS ≥ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	2.99	3.59	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient		[1]	-	25	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information

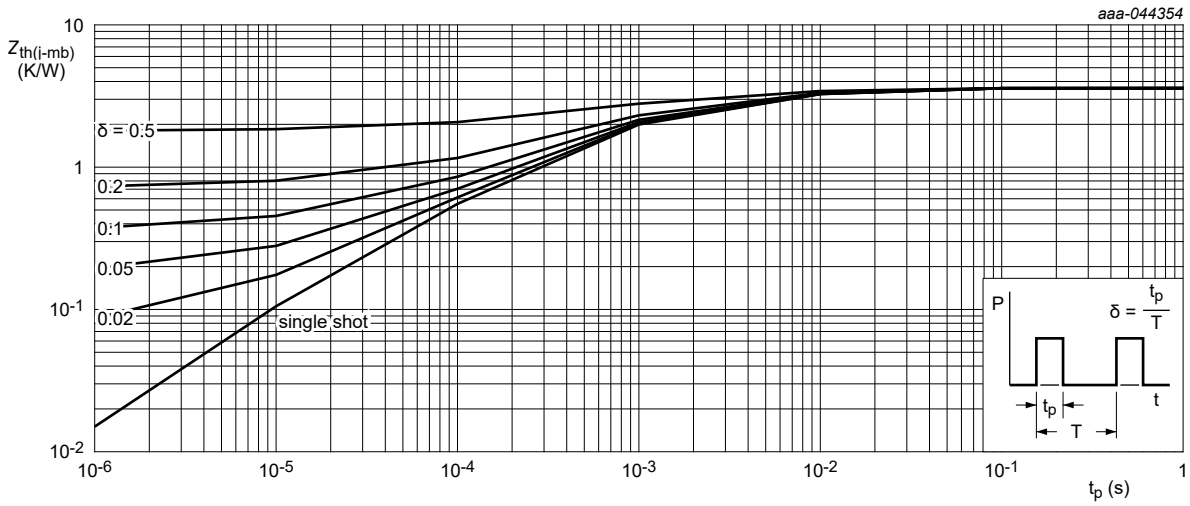


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		-	30	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 8		1.2	1.7	2.2	V
		I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = 150 °C		-	1	-	V
		I_D = 0.25 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	2.1	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-6	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C		-	100	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

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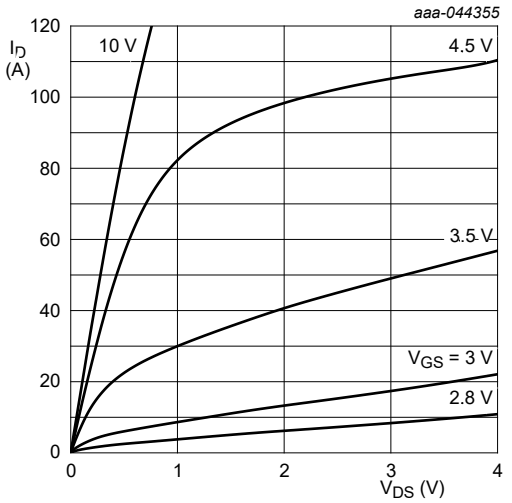
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	5.7	7.1	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 150 °C; Fig. 10		-	-	11.7	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; Fig. 9		-	7.8	10.5	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 150 °C; Fig. 10		-	-	17.3	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	6.9	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 11; Fig. 12		-	5	-	nC
		I_D = 10 A; V_{DS} = 15 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 11; Fig. 12		-	10.6	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	10	-	nC
Q_{GS}	gate-source charge	I_D = 10 A; V_{DS} = 15 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 11; Fig. 12		-	2.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	1	-	nC
Q_{GD}	gate-drain charge			-	1.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 15 V; T_j = 25 °C; Fig. 11; Fig. 12		-	3	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 13		-	673	-	pF
C_{oss}	output capacitance			-	420	-	pF
C_{rss}	reverse transfer capacitance			-	26	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 1.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	8.4	-	ns
t_r	rise time			-	20.2	-	ns
$t_{d(off)}$	turn-off delay time			-	9.4	-	ns
t_f	fall time			-	12	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C		-	9.4	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 14		-	0.75	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V; T_j = 25 °C; Fig. 15		-	13.3	-	ns
Q_r	recovered charge		[1]	-	3.3	-	nC

[1] includes capacitive recovery

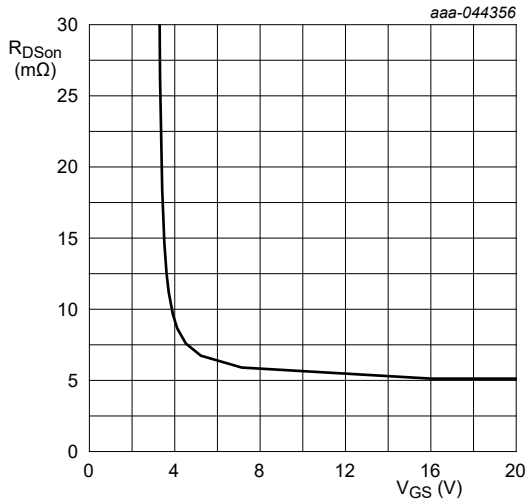
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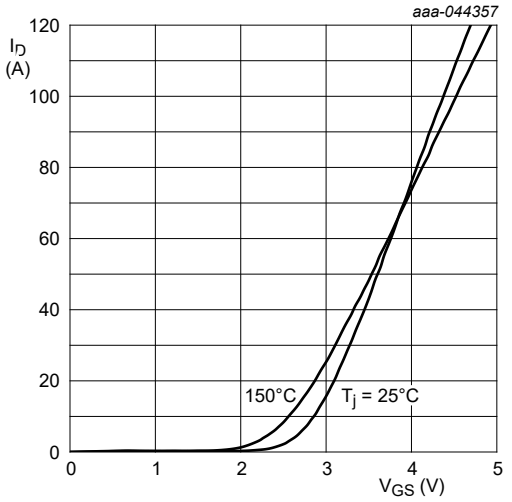
T_j = 25 °C

Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values



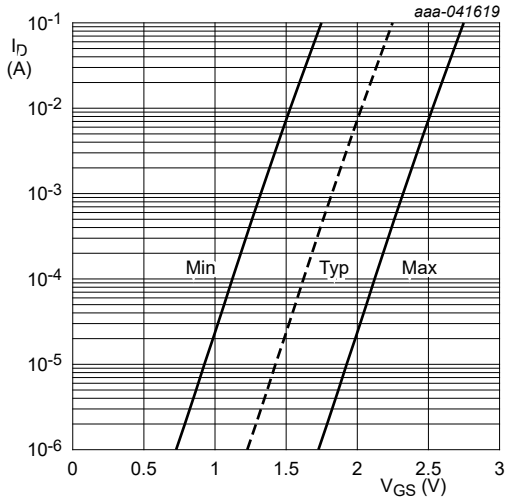
T_j = 25 °C; I_D = 10 A

Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



V_{DS} = 8 V

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

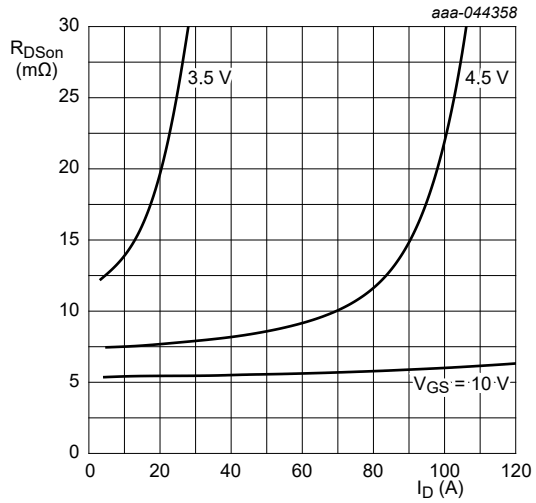


T_j = 25 °C; V_{DS} = 5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage

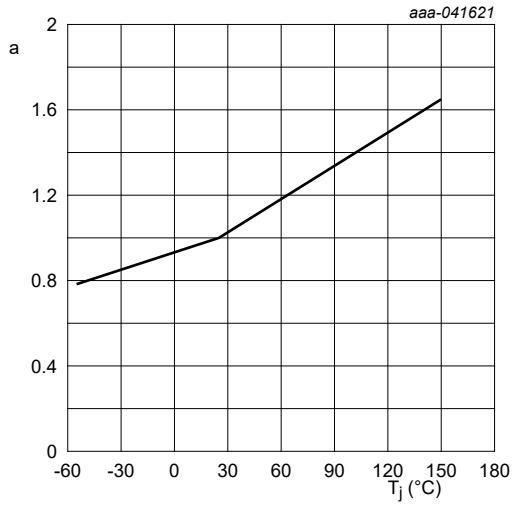
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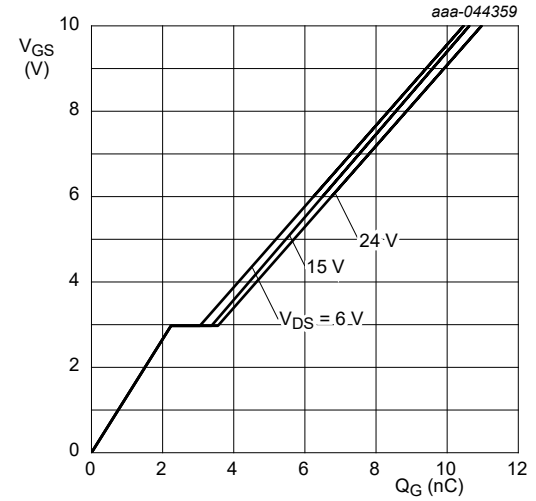
T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 10 A

Fig. 11. Gate-source voltage as a function of gate charge; typical values

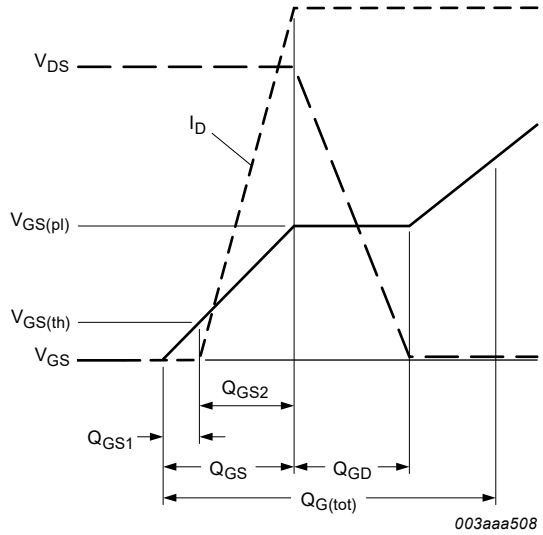
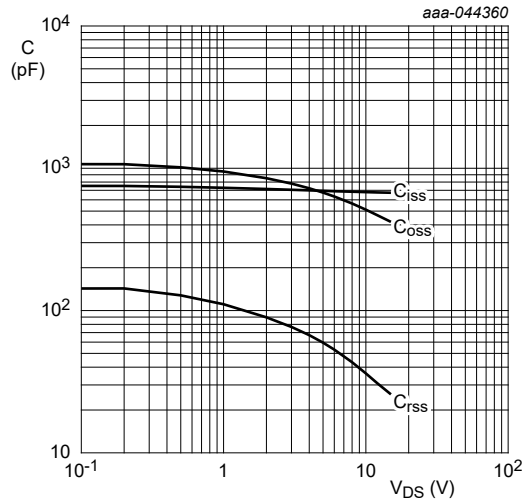


Fig. 12. Gate charge waveform definitions

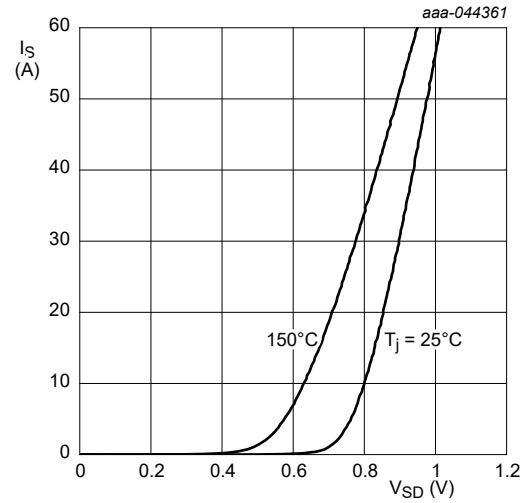
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V_{GS} = 0 V; f = 1 MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

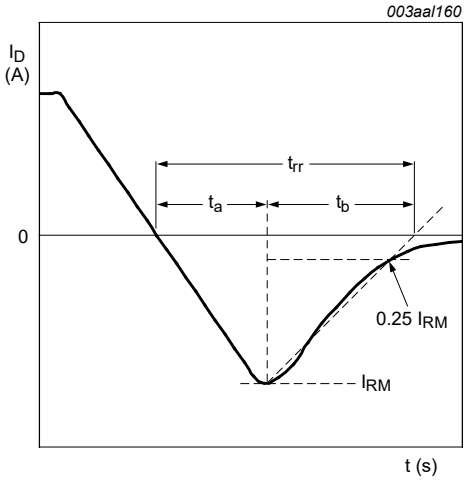
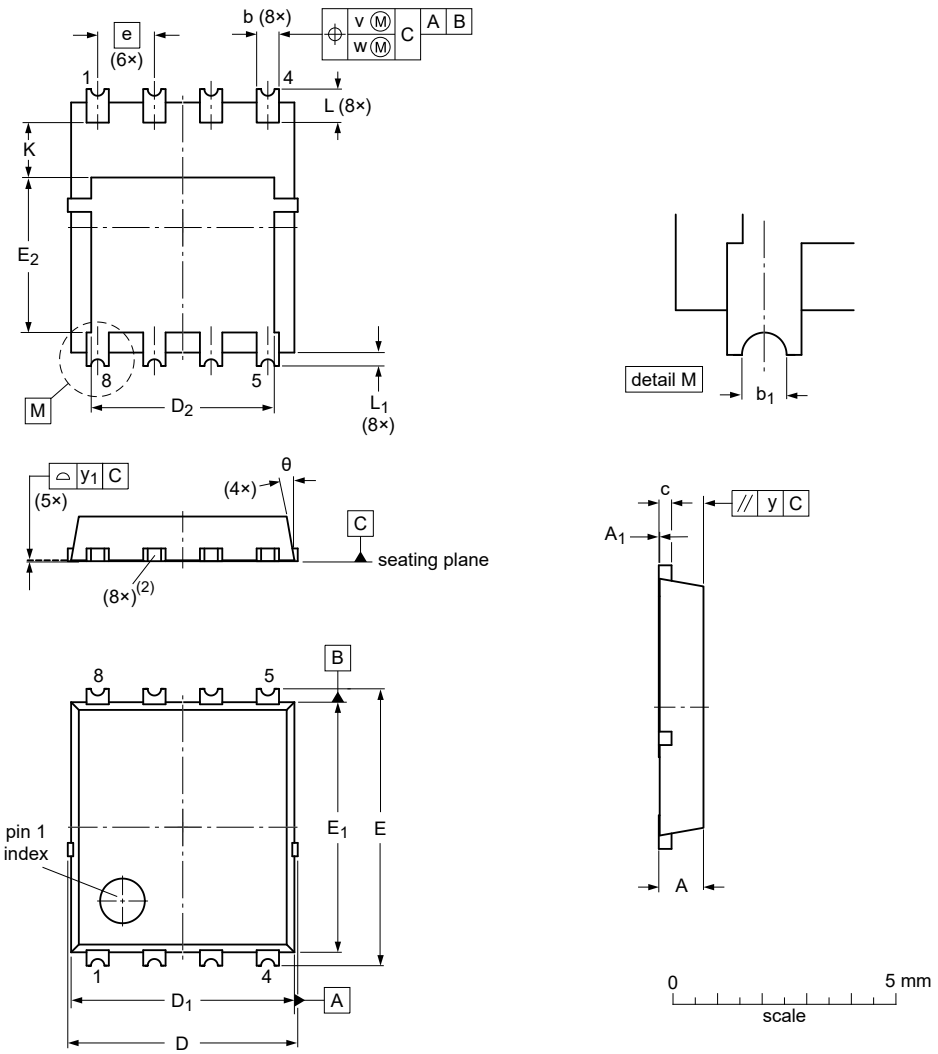


Fig. 15. Reverse recovery timing definition

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11. Package outline

MLPAK56-WF: 8 terminals; body 5.15 x 6.2 x 1.0 mm **SOT8038-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1 [2]	c	D	D_1 [1]	D_2	E	E_1 [1]	E_2	e	K	L	L_1	v	w	y	θ
	max	1.1	0.05	0.67		0.33		5.15	4.25	6.35	5.75	3.67		-	0.85	0.4				12°
mm	nom	1.0	-	-	0.2 REF	0.28	5.15 REF	5.00	4.10	6.20	5.60	3.47	1.27	-	0.75	-	0.1	0.05	0.1	-
	min	0.9	0.00	0.57		0.23		4.85	3.95	6.05	5.45	3.27		1.1	0.65	0.2				0°

Notes:
1. Dimensions do not include mold flash, plastic protrustions, metal protrustions, or gate burrs. Mold flash or gate burr shall not exceed 0.15 mm per end.
2. Side-wettable flanks.

sot8038-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8038-2						~~23-08-25~~ 24-10-28

Fig. 16. Package outline MLPAK56-WF (SOT8038-2)

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12. Soldering

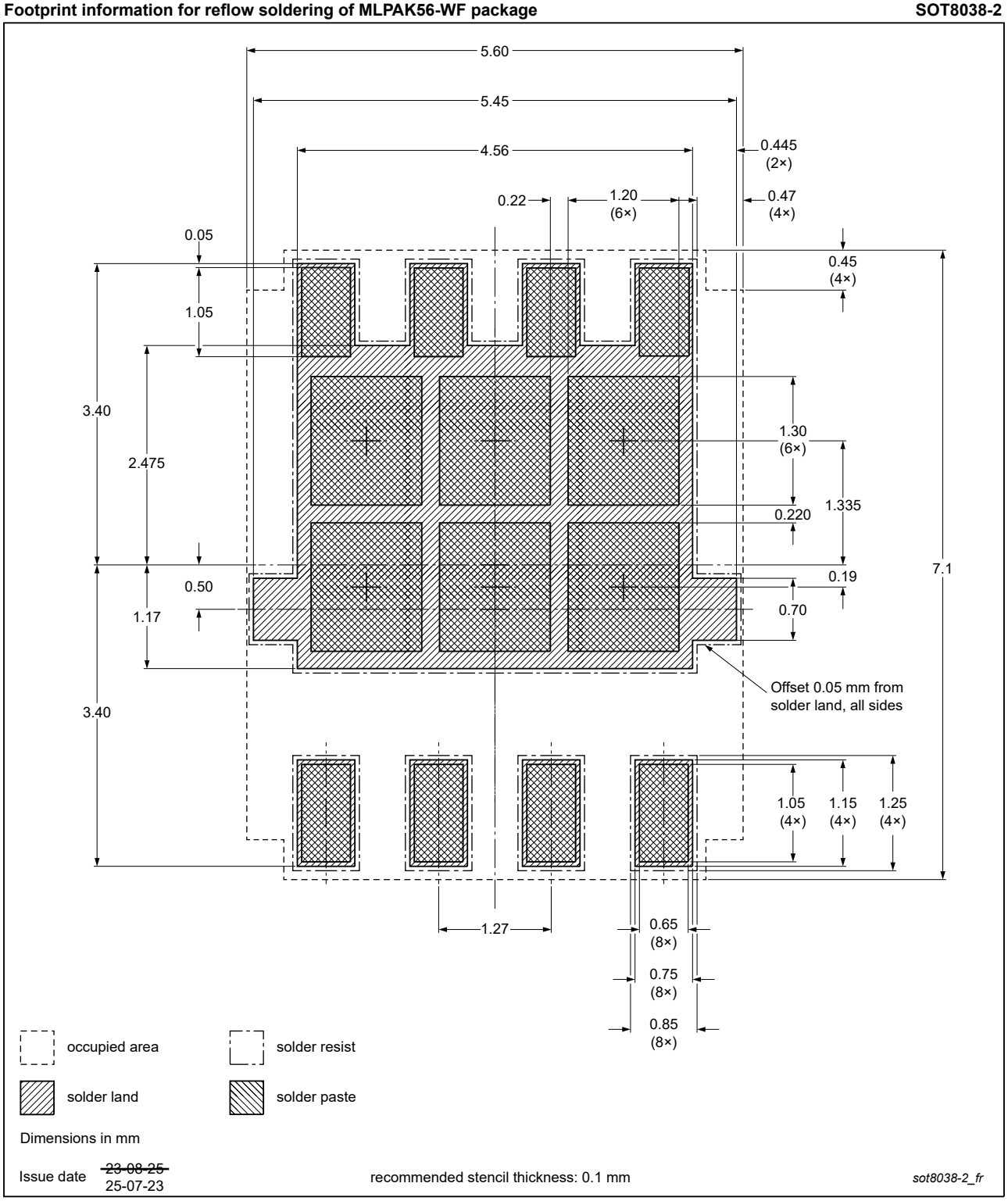


Fig. 17. Reflow soldering footprint for MLPAK56-WF (SOT8038-2)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 29 January 2026