



PXN7R0-30QLA

N-channel 30 V, 7.0 mOhm, logic level Trench MOSFET in MLPAK33

16 October 2025

Product data sheet

1. General description

General purpose MOSFET for standard applications, 55 A, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Battery Management System
- Motor drive
- Load switching

4. Quick reference data

Table 1. Quick reference data

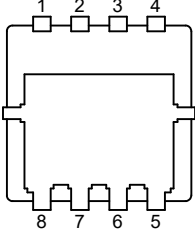
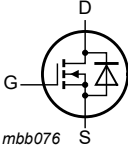
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C		-	-	30	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	55	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	35	W
T _j	junction temperature			-55	-	150	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	5.9	7	mΩ
		V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	8.7	10.5	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C; Fig. 11 ; Fig. 12		-	1.1	-	nC
Q _{G(tot)}	total gate charge			-	4.9	-	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 18.2 A; V _{sup} ≤ 30 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	[1]	-	-	33.1	mJ
Source-drain diode							
Q _r	recovered charge	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 15 V; T _j = 25 °C; Fig. 15	[2]	-	4.1	-	nC

[1] Protected by 100% test

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN7R0-30QLA	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN7R0-30QLA	7AV

8. Limiting values

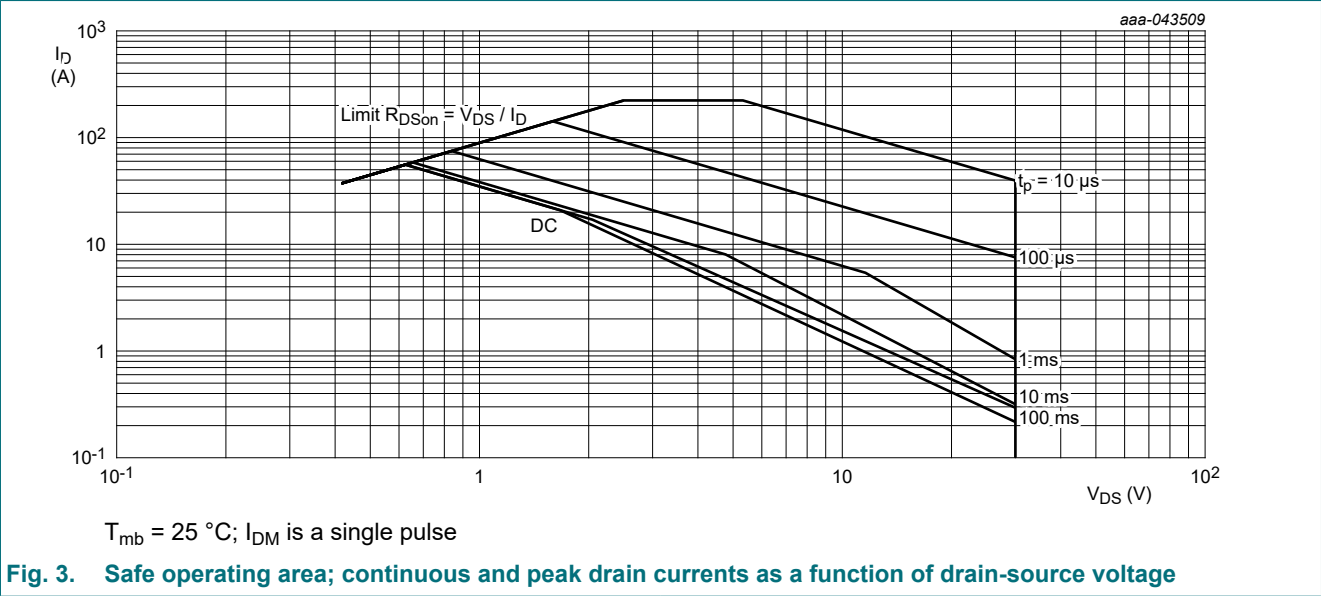
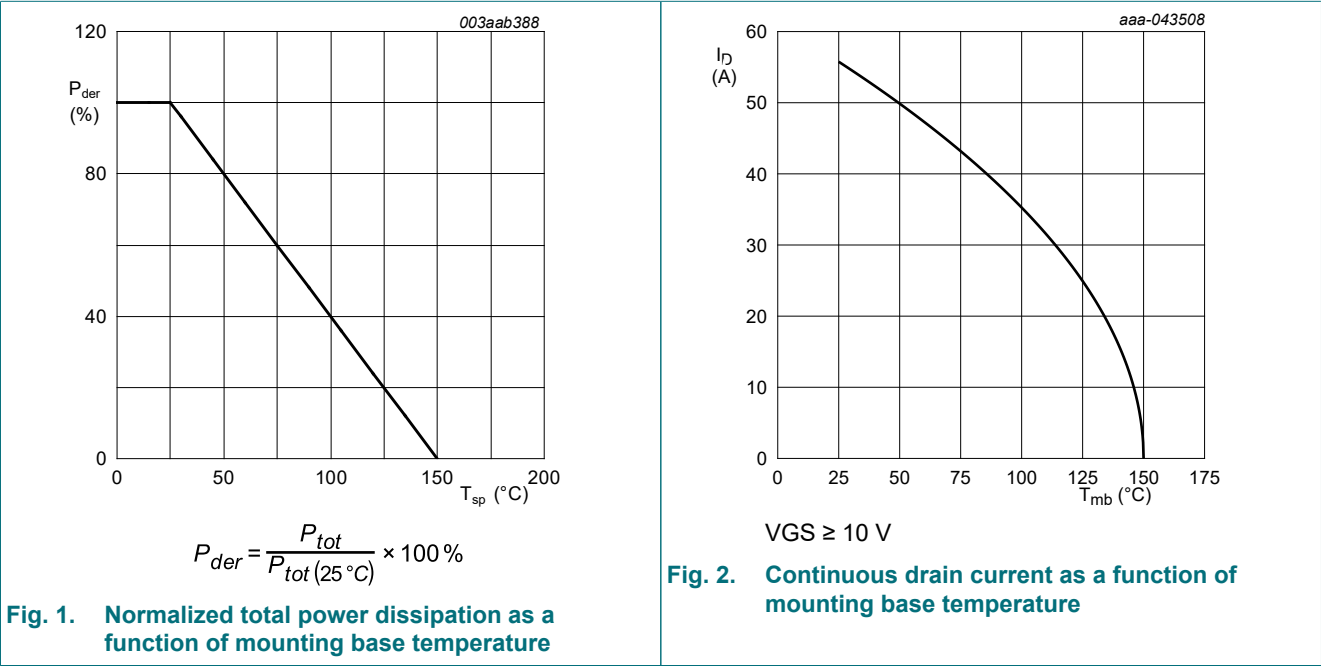
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	30	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	35	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	55	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	35	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	223	A
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	29	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	223	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 18.2\text{ A}$; $V_{sup} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped	[1]	-	33.1	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$	[1]	-	18.2	A

[1] Protected by 100% test



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	2.99	3.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	145	185	K/W
			[2]	-	55	70	K/W
		in free air; $t \leq 5$ s	[2]	-	21	26	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

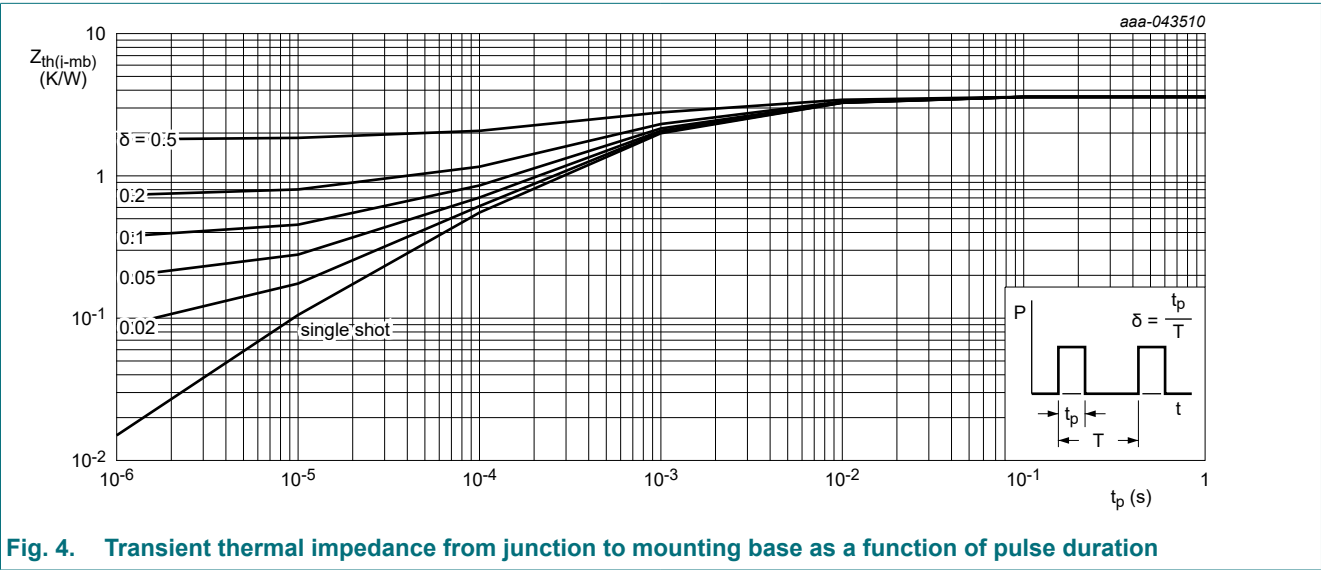


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		30	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = -55\text{ }^\circ\text{C}$		-	30	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 8		1.2	1.8	2.2	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 150\text{ }^\circ\text{C}$		-	1	-	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = -55\text{ }^\circ\text{C}$		-	2.2	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$		-	-6.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	0.02	1	μA
		$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$		-	100	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA

N-channel 30 V, 7.0 mOhm, logic level Trench MOSFET in MLPAK33

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9		-	5.9	7	mΩ
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$; Fig. 10		-	-	11.6	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9		-	8.7	10.5	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$; Fig. 10		-	-	17.3	mΩ
R_G	gate resistance	$f = 1\text{ MHz}; T_j = 25\text{ }^{\circ}\text{C}$		-	5	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 10\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 12		-	4.9	-	nC
		$I_D = 10\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 12		-	10.6	-	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$		-	9.9	-	nC
Q_{GS}	gate-source charge	$I_D = 10\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 12		-	2.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	1.2	-	nC
Q_{GD}	gate-drain charge			-	1.1	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10\text{ A}; V_{DS} = 15\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 ; Fig. 12		-	3.2	-	V
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 13		-	683	-	pF
C_{oss}	output capacitance			-	384	-	pF
C_{rss}	reverse transfer capacitance			-	22	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 1.5\text{ }^{\circ}\Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ }^{\circ}\Omega; T_j = 25\text{ }^{\circ}\text{C}$		-	8.3	-	ns
t_r	rise time			-	14.1	-	ns
$t_{d(off)}$	turn-off delay time			-	9.1	-	ns
t_f	fall time			-	9.3	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^{\circ}\text{C}$		-	8.9	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14		-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15		-	14.6	-	ns
Q_r	recovered charge		[1]	-	4.1	-	nC

[1] includes capacitive recovery

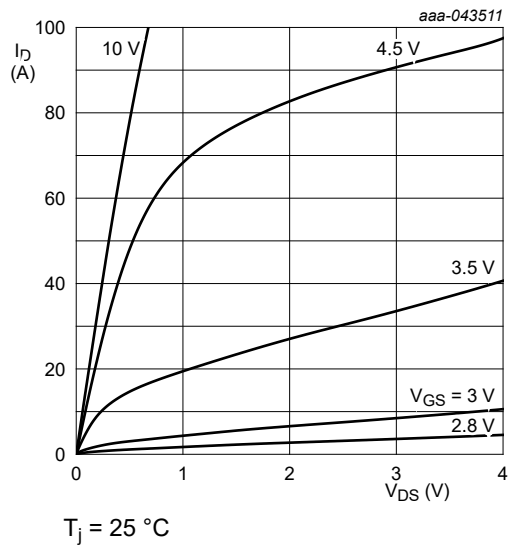


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

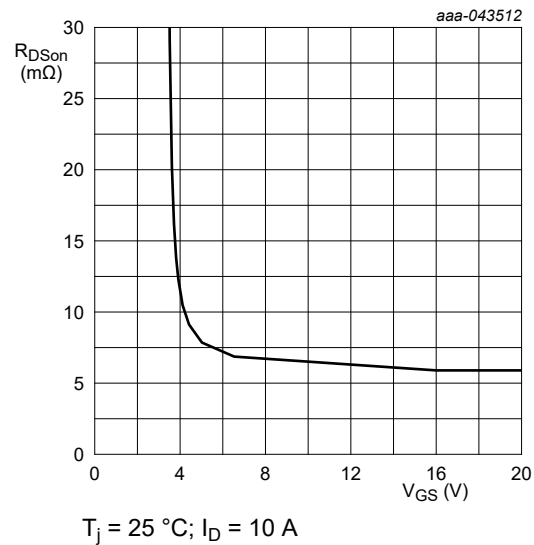


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

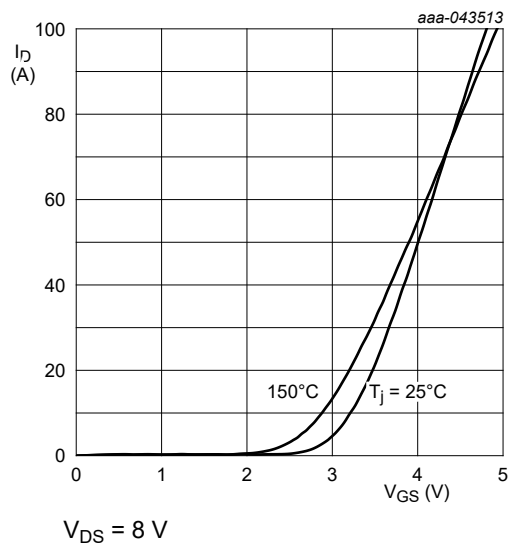


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

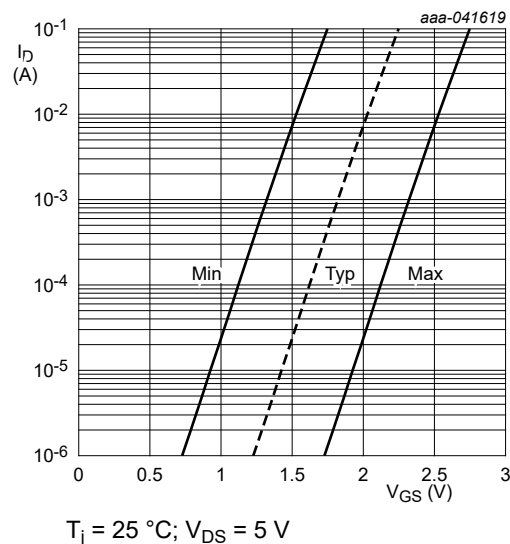


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

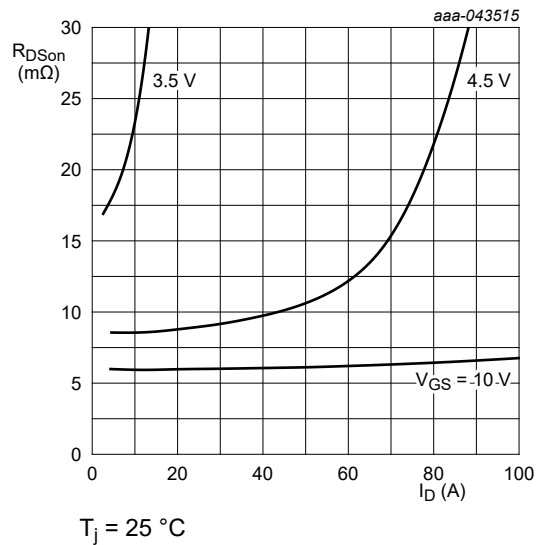


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

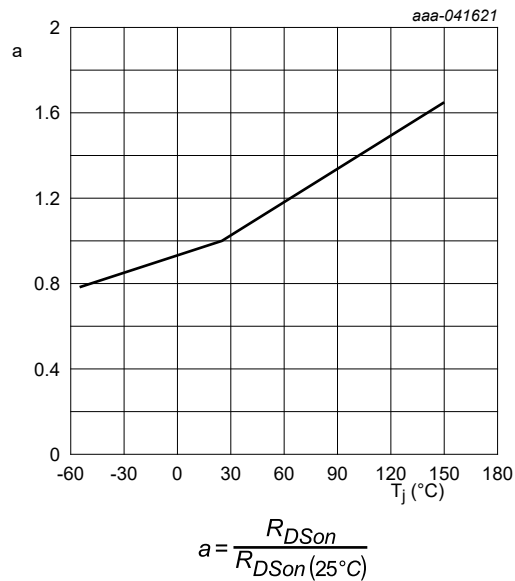


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

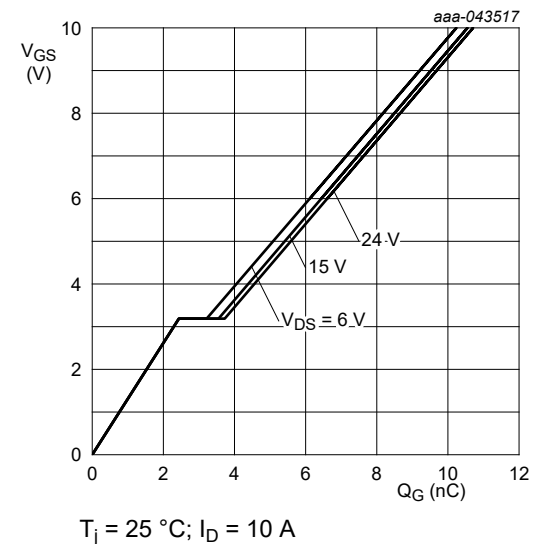


Fig. 11. Gate-source voltage as a function of gate charge; typical values

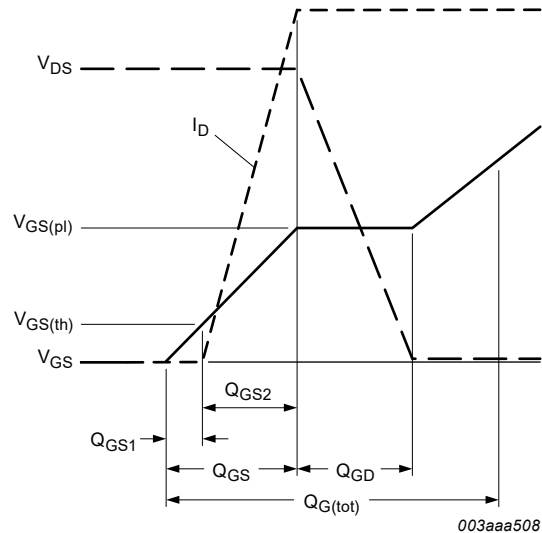


Fig. 12. Gate charge waveform definitions

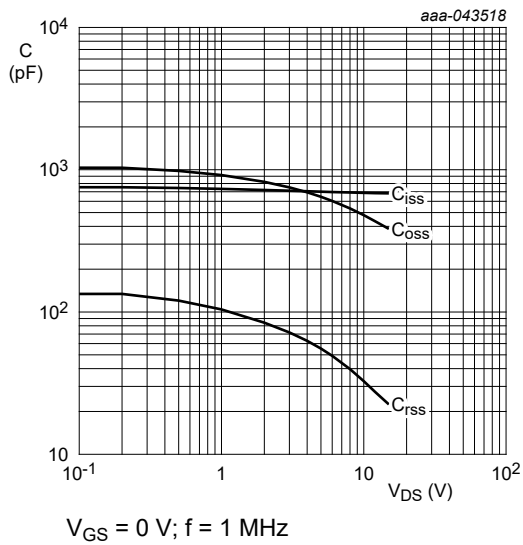


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

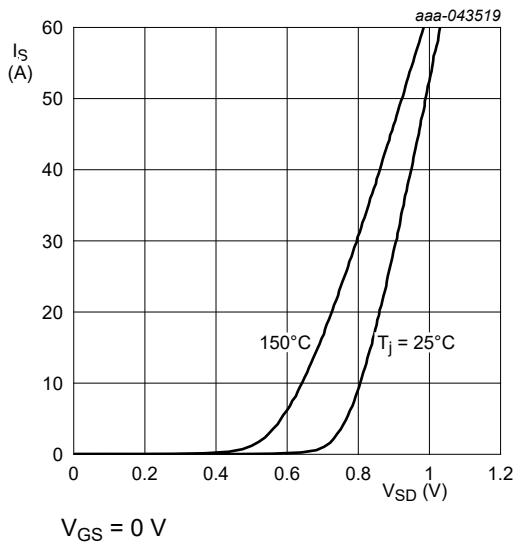


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

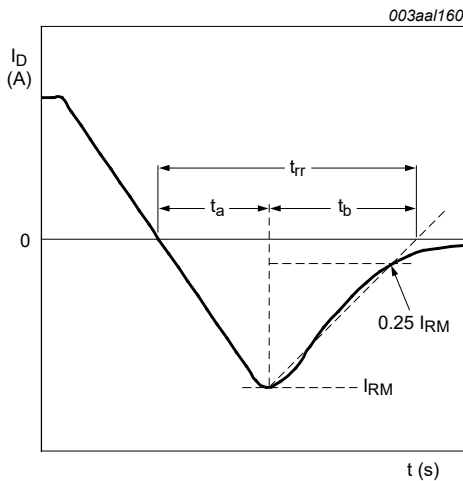


Fig. 15. Reverse recovery timing definition

11. Package outline

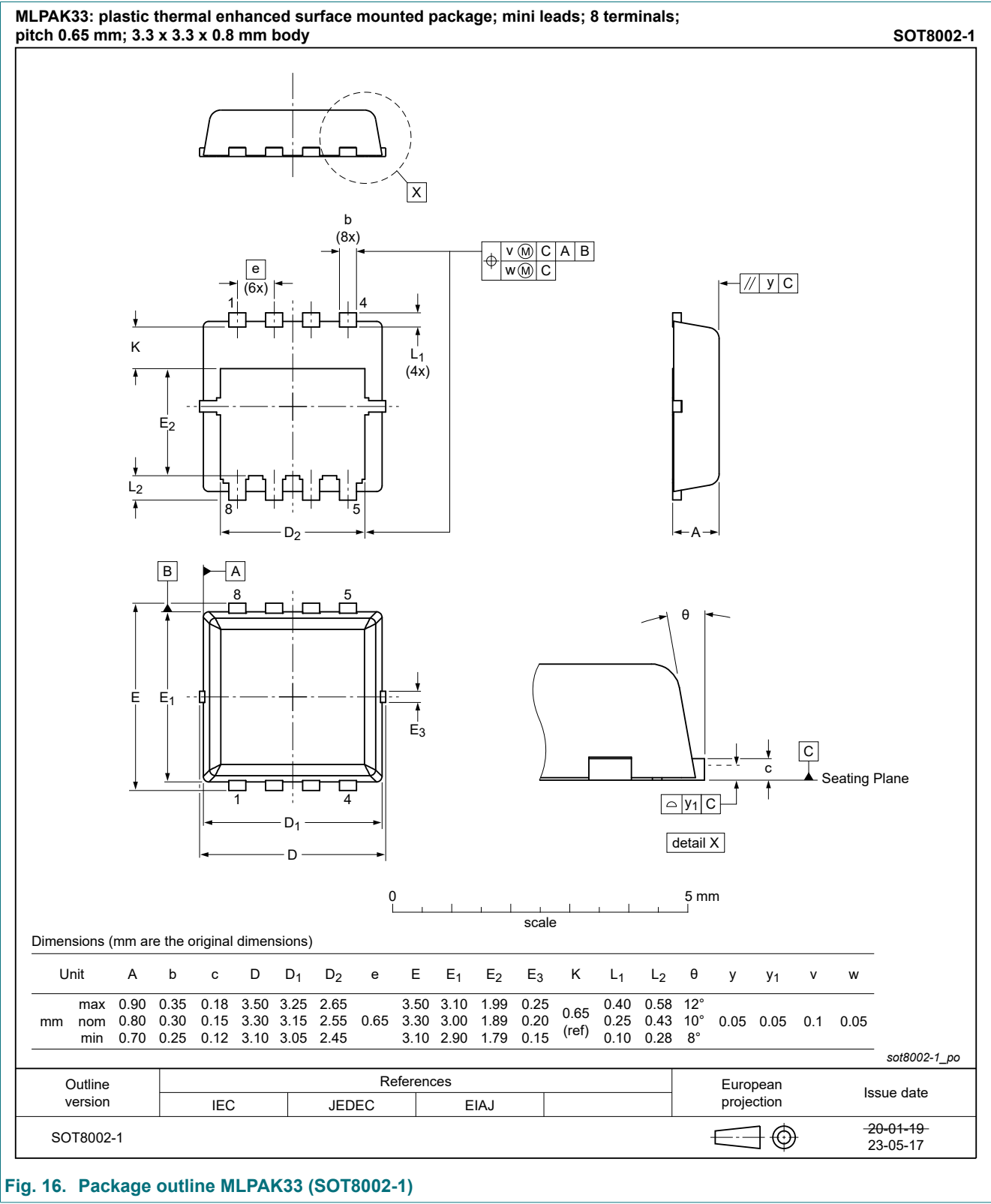


Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

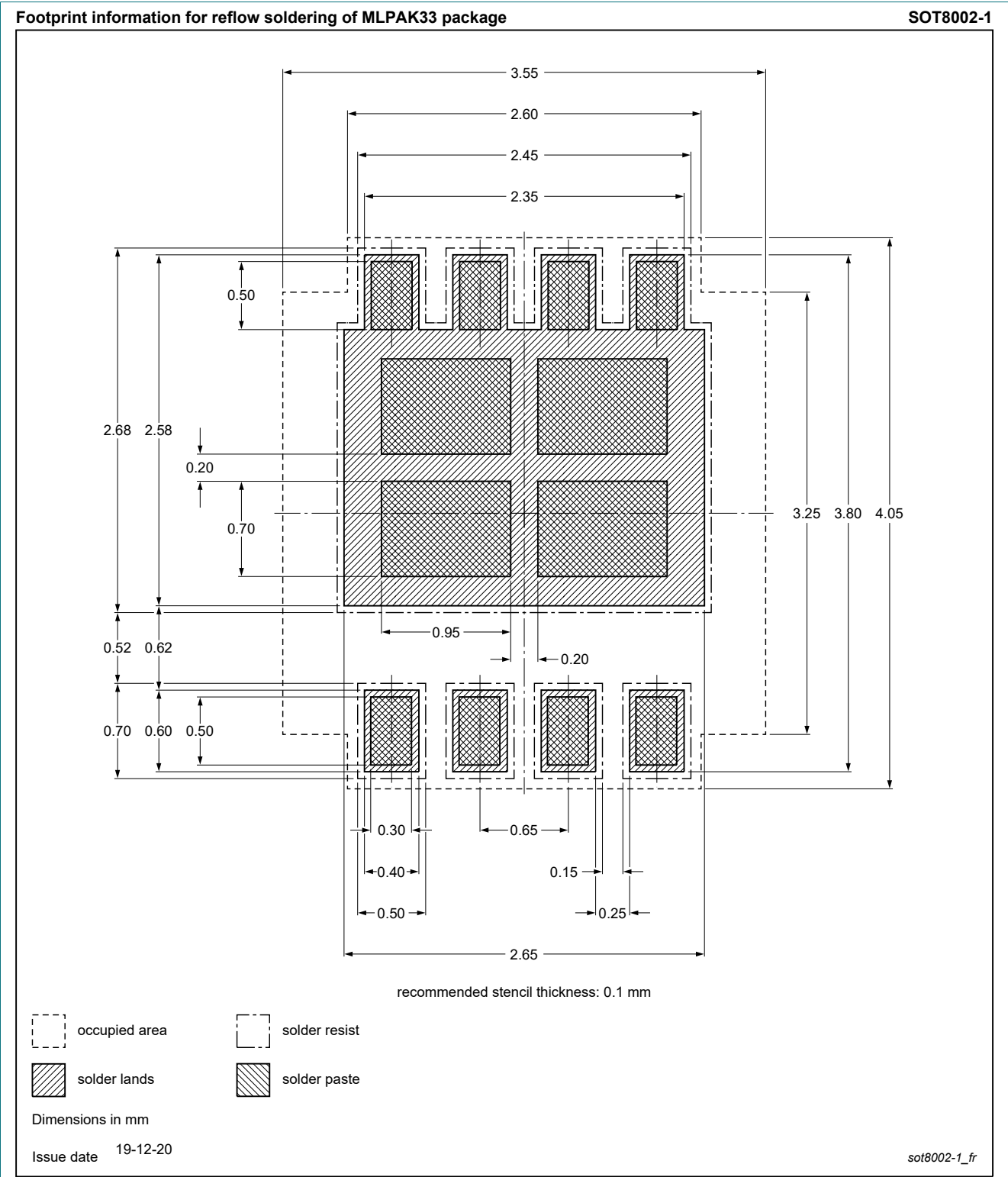


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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