PSMNS6R5-40MYX8

40 V, 6.5 mΩ, Standard Level N-channel MOSFET in MLPAK56-WF Package

Rev. 1 — 21 October 2026 Product data sheet

1. General Description

40 V, N-Channel MOSFET with standard level gate drive. Qualified to 175 °C and meet JEDEC for industrial requirements delivering high performance and reliability.

2. Features and Benefits

- 175 °C rating junction temperature
- Reduced cell-pitch wafer design
- Industry-standard 5 x 6 mm SO8 footprint (30 mm^2) with side wettable pins
- MLPAK half copper clip technology:
  - Reduced R_{th}, $R_{DS(ON)}$, and package inductance
  - Increase maximum current capability and improve current spreading
- Suitable for industrial and consumer power applications

3. Applications

- High-performance power switching
- Synchronous rectification
- Brushed and Brushless DC motor control
- Battery management systems (BMS)
- eFuse
- Load-switch

4. Quick Reference Data

Table 1. Quick Reference Data

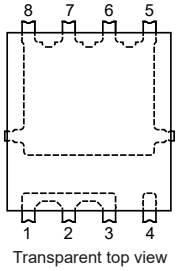
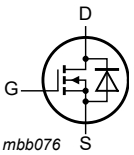
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2 [1]	-	-	75	A
Static Characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12	4.13	5.9	6.5	mΩ
Dynamic Characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14	-	12.1	14.5	nC

[1] Application tests show a continuous current of 75 A. The PCB, the thermal design, and the operating temperature limit the actual current.

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5. Pinning Information

Table 2. Pinning Information

Pin	Symbol	Description	Simplified Outline	Graphic Symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering Information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNS6R5-40MYX8	MLPAK56	Plastic, thermal enhanced surface mounted package with side-wettable flanks (SWF); minileads; 8 terminals; pitch 1.27 mm; 5.6 × 5.15 × 1.0 mm body	SOT8038-4

7. Marking

Table 4. Marking Codes

Type Number	Marking Code
PSMNS6R5-40MYX8	PN6S504 X8MY

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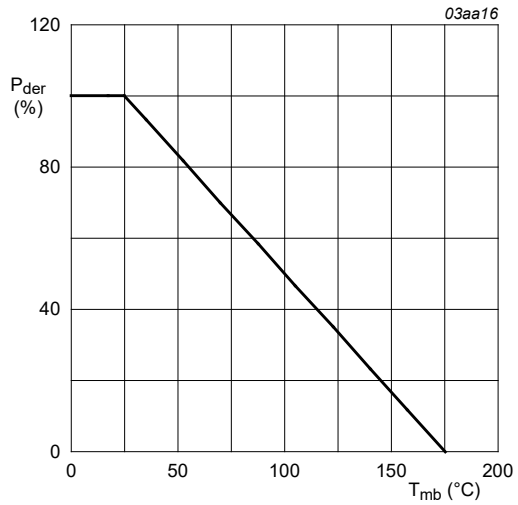
8. Limiting Values

Table 5. Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C, unless otherwise specified.

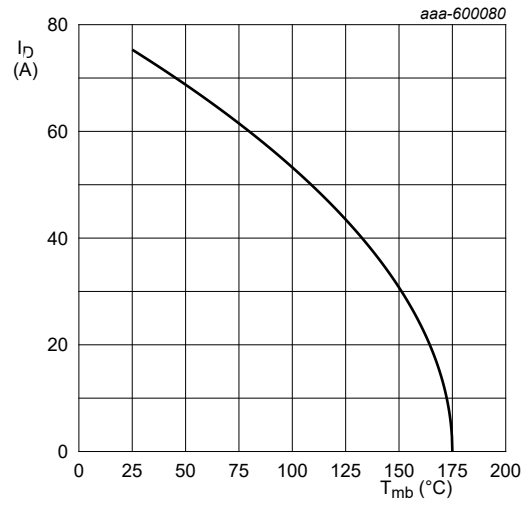
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	40	V
V_{GS}	gate-source voltage		−20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1	-	72	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2 [1]	-	75	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2	-	53.3	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3 [1]	-	231	A
T_{stg}	storage temperature		−55	175	°C
T_j	junction temperature		−55	175	°C
Source-drain Diode					
I_S	source current	T_{mb} = 25 °C [1]	-	75	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C	-	231	A
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 21 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	42	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	-	75	A

[1] Application tests show a continuous current of 75 A. The PCB, the thermal design, and the operating temperature limit the actual current.



$$P_{der} = \frac{P_{tot}}{P_{tot(25\ °C)}} \times 100\ \%$$

Fig. 1. Normalized Total Power Dissipation as a Function of Mounting Base Temperature



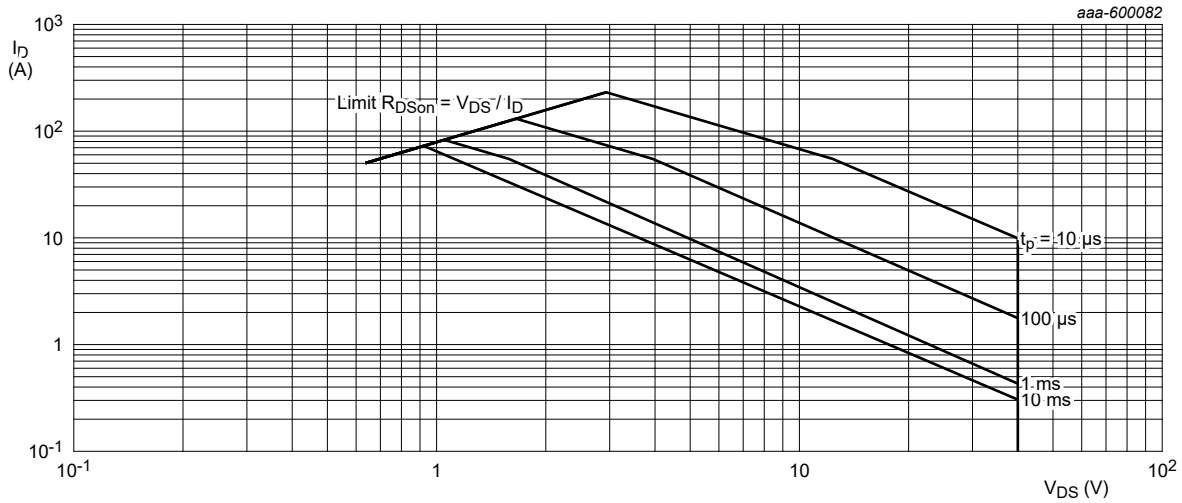
V_{GS} ≥ 10 V

This current will be demonstrated during product characterisation. The PCB, the thermal design, and the operating temperature limit the actual current.

Fig. 2. Continuous Drain Current as a Function of Mounting Base Temperature

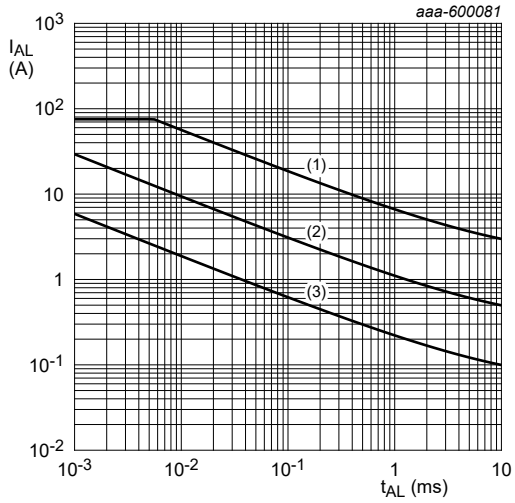
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T_{mb} = 25 °C; I_{DM} is a single pulse.

Fig. 3. Safe Operating Area; Continuous and Peak Drain Currents as a Function of Drain-source Voltage



- (1) $T_{j(init)}$ = 25 °C
- (2) $T_{j(init)}$ = 150 °C
- (3) Repetitive Avalanche

Fig. 4. Avalanche Rating; Avalanche Current as a Function of Avalanche Time

9. Thermal Characteristics

Table 6. Thermal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base		-	1.61	2.09	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient[1]		-	24	-	K/W

[1] The device is placed on a 2s2p FR4 PCB as defined by the JEDEC standards (JESD51-5, -7). The PCB is placed vertically in still air.

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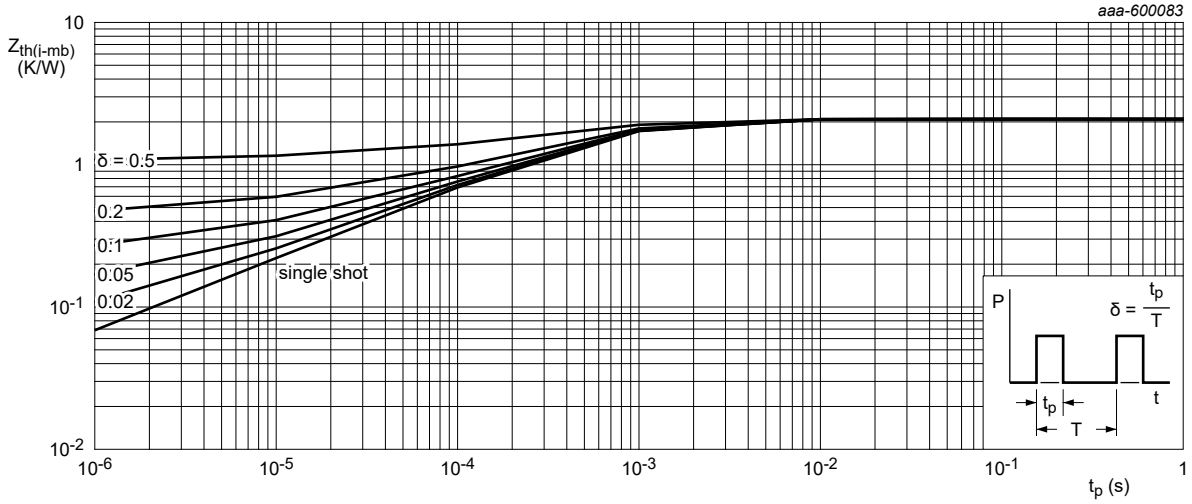


Fig. 5. Transient Thermal Impedance from Junction to Mounting Base as a Function of Pulse Duration

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10. Characteristics

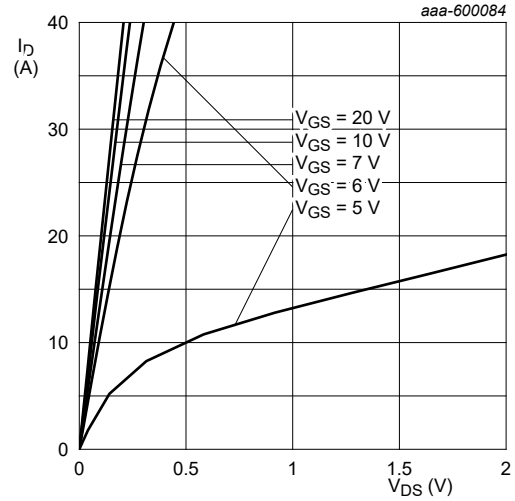
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	44.9	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = −40 °C	-	43.6	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = −55 °C	36	42	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10	2.3	3	3.7	V
		I_D = 0.1 mA; V_{DS} = V_{GS}; T_j = −55 °C; Fig. 10	-	-	4.1	V
		I_D = 0.1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10	1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C	-	1	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	50	200	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	5	100	nA
		V_{GS} = −20 V; V_{DS} = 0 V; T_j = 25 °C	-	5	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11	4.13	5.9	6.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 12	5.67	8.1	9.1	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 12	6.16	8.8	9.7	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12	7.35	10.5	11.6	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C	0.5	1.25	2.0	Ω
Dynamic Characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14	-	12.1	14.5	nC
Q_{GS}	gate-source charge		-	3.4	5.1	nC
Q_{GD}	gate-drain charge		-	2.3	3.5	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15	-	800	1200	pF
C_{oss}	output capacitance		-	232	350	pF
C_{rss}	reverse transfer capacitance		-	6.8	10.5	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C	-	9	-	ns
t_r	rise time		-	2.5	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns
t_f	fall time		-	3	-	ns
Source-drain Diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16	-	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; di_S/dt = −100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17 [1]	-	26	-	ns
Q_r	recovered charge		-	19	-	nC

[1] Includes capacitive recovery

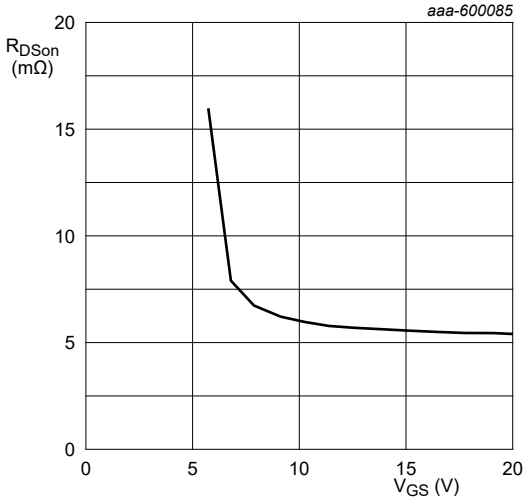
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T_j = 25 °C

Fig. 6. Output Characteristics; Drain Current as a Function of Drain-source Voltage; Typical Values



T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source On-state Resistance as a Function of Gate-source Voltage; Typical Values

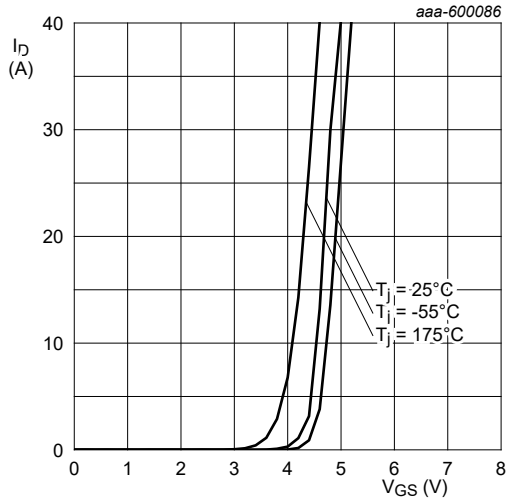
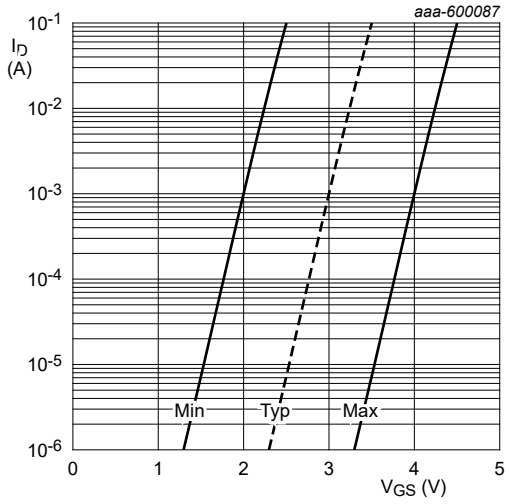


Fig. 8. Transfer Characteristics; Drain Current as a Function of Gate-source Voltage; Typical Values

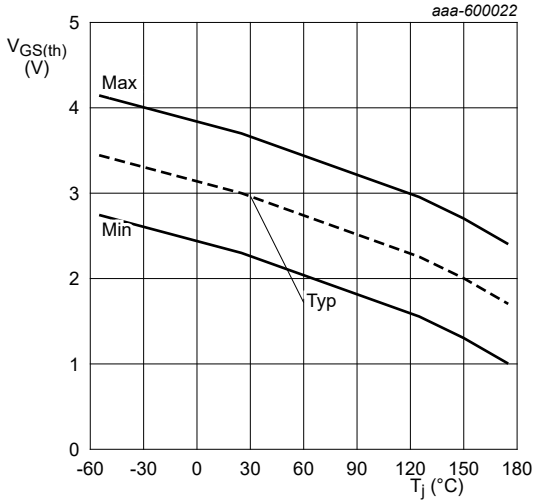


T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold Drain Current as a Function of Gate-source Voltage

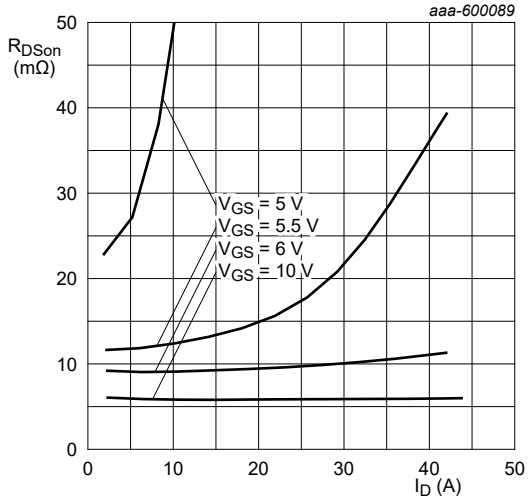
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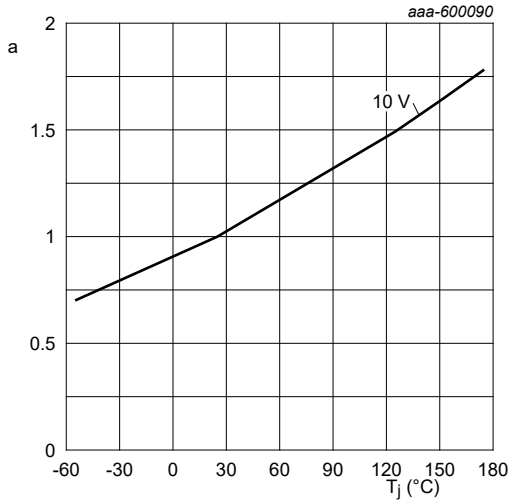
I_D = 0.1 mA; V_{DS} = V_{GS}

Fig. 10. Gate-source Threshold Voltage as a Function of Junction Temperature



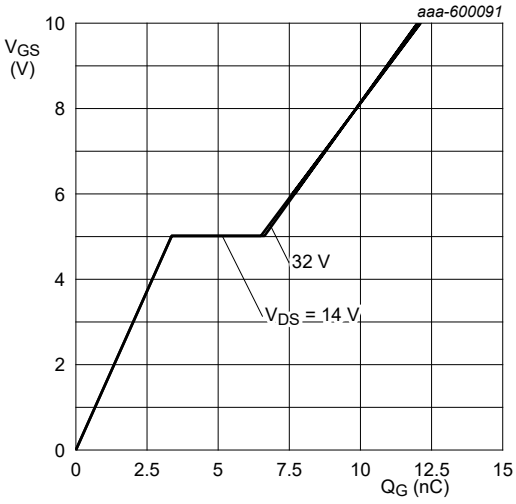
T_j = 25 °C

Fig. 11. Drain-source On-state Resistance as a Function of Drain Current; Typical Values



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\,°C)}}$$

Fig. 12. Normalized Drain-source On-state Resistance Factor as a Function of Junction Temperature



T_j = 25 °C; I_D = 25 A

Fig. 13. Gate-source Voltage as a Function of Gate Charge; Typical Values

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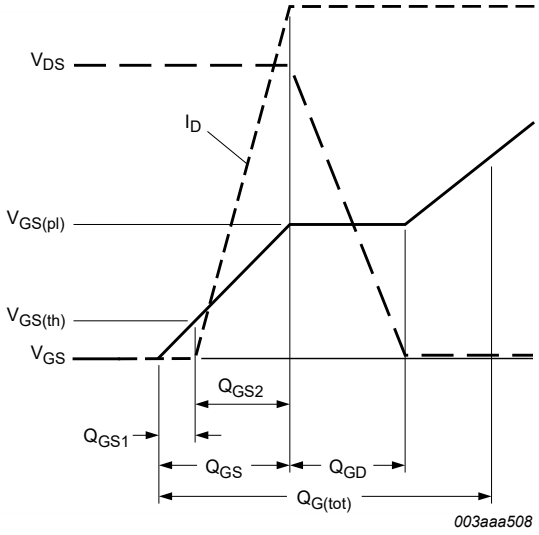
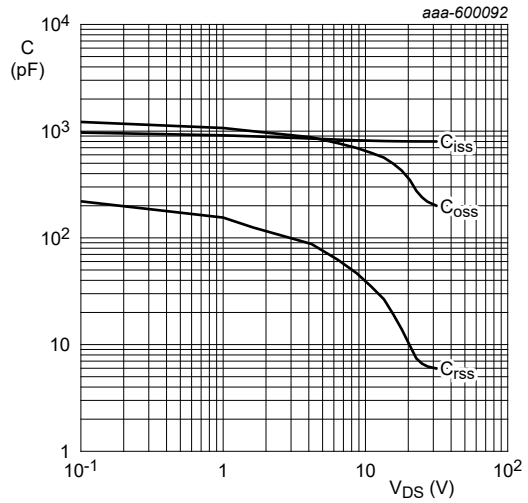
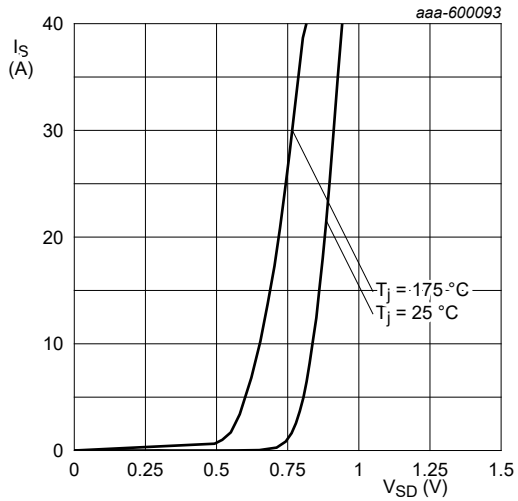


Fig. 14. Gate Charge Waveform Definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, Output, and Reverse Transfer Capacitances as a Function of Drain-source Voltage; Typical Values



V_{GS} = 0 V

Fig. 16. Source-drain (Diode Forward) Current as a Function of Source-drain (Diode Forward) Voltage; Typical Values

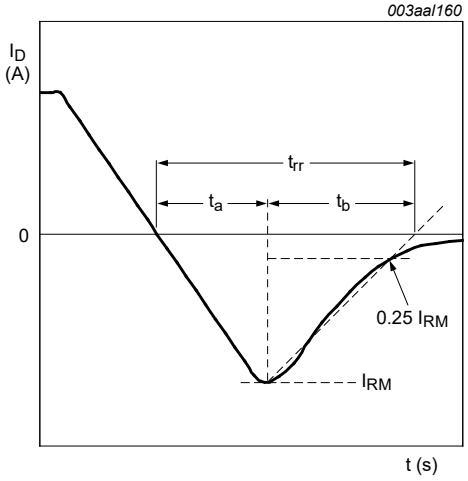


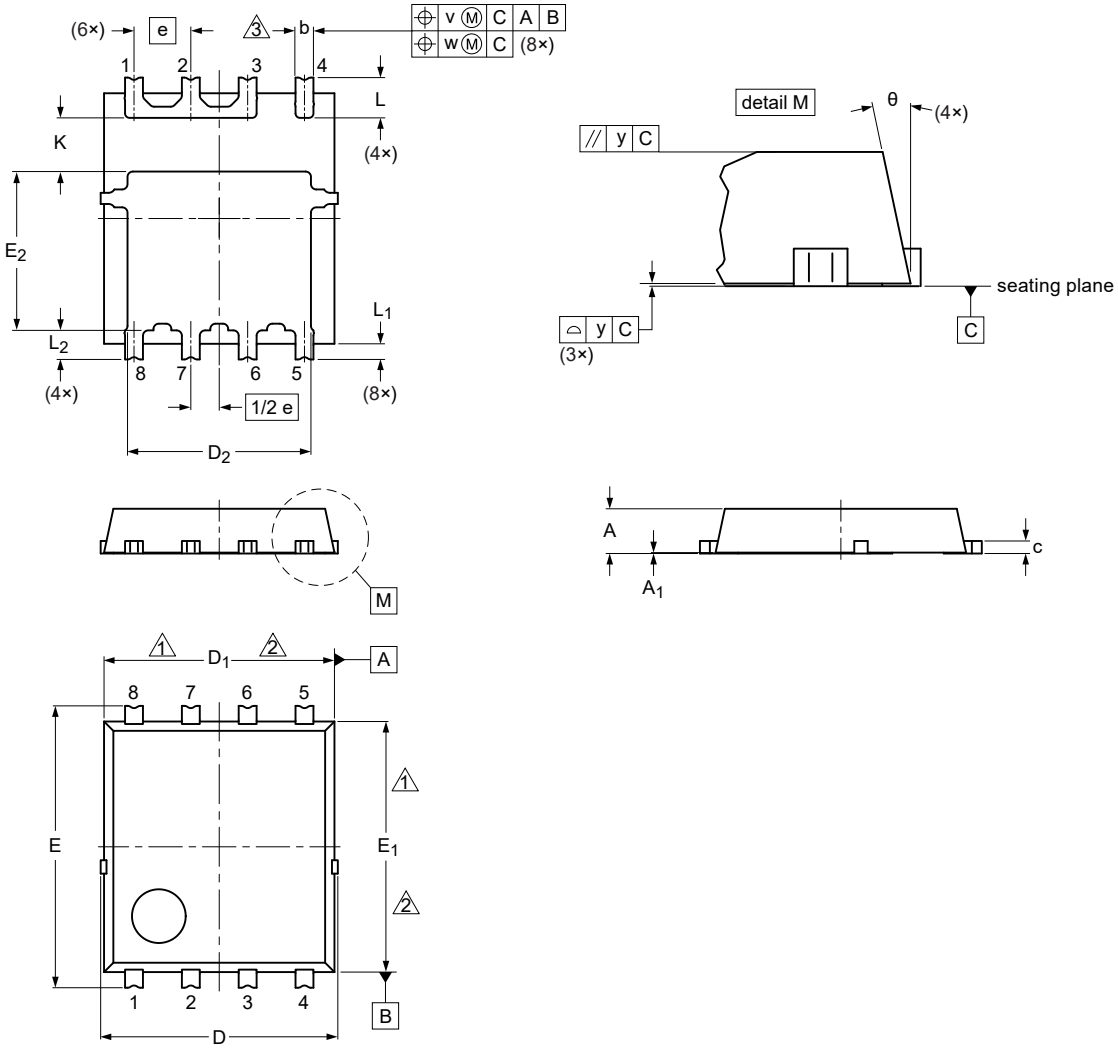
Fig. 17. Reverse Recovery Timing Definition

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11. Package Outline

MLPAK56: Plastic, thermal enhanced surface mounted package with side-wettable flanks (SWF); minileads; 8 terminals; pitch 1.27 mm; 5.6 x 5.15 x 1.0 mm body **SOT8038-4**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	c	D	D_1	D_2	E	E_1	E_2	e	K	L	L_1	L_2	v	w	y	θ
mm	max	1.1	0.05	0.52	0.33	5.45	5.25	4.25	6.45	5.75	3.65	1.27 BSC	1.2 REF	1.00	0.35 REF	0.75	0.1	0.05	0.1	12°
	nom	1.0			0.28		5.15	4.10	6.30	5.60	3.55			0.90		0.65				
	min	0.9	0	0.34	0.23	5.15	5.05	3.95	6.15	5.45	3.45			0.80		0.55				0°

Note
1. Dimension does not include mold flash, plastic protrusion or gate burrs. These shall not exceed 0.15 mm per end.
2. Dimension does not include interterminal flash or protrusion which shall not exceed 0.25 mm per side.
3. Dimension does not include metal protrusion or burr which shall not exceed 0.075 mm per lead side.

sot8038-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8038-4						24-12-12

Fig. 18. Package Outline MLPAK56 (SOT8038-4)

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12. Soldering

Table 8. Soldering

Footprint information for reflow soldering of MLPAK56 package	SOT8038-4

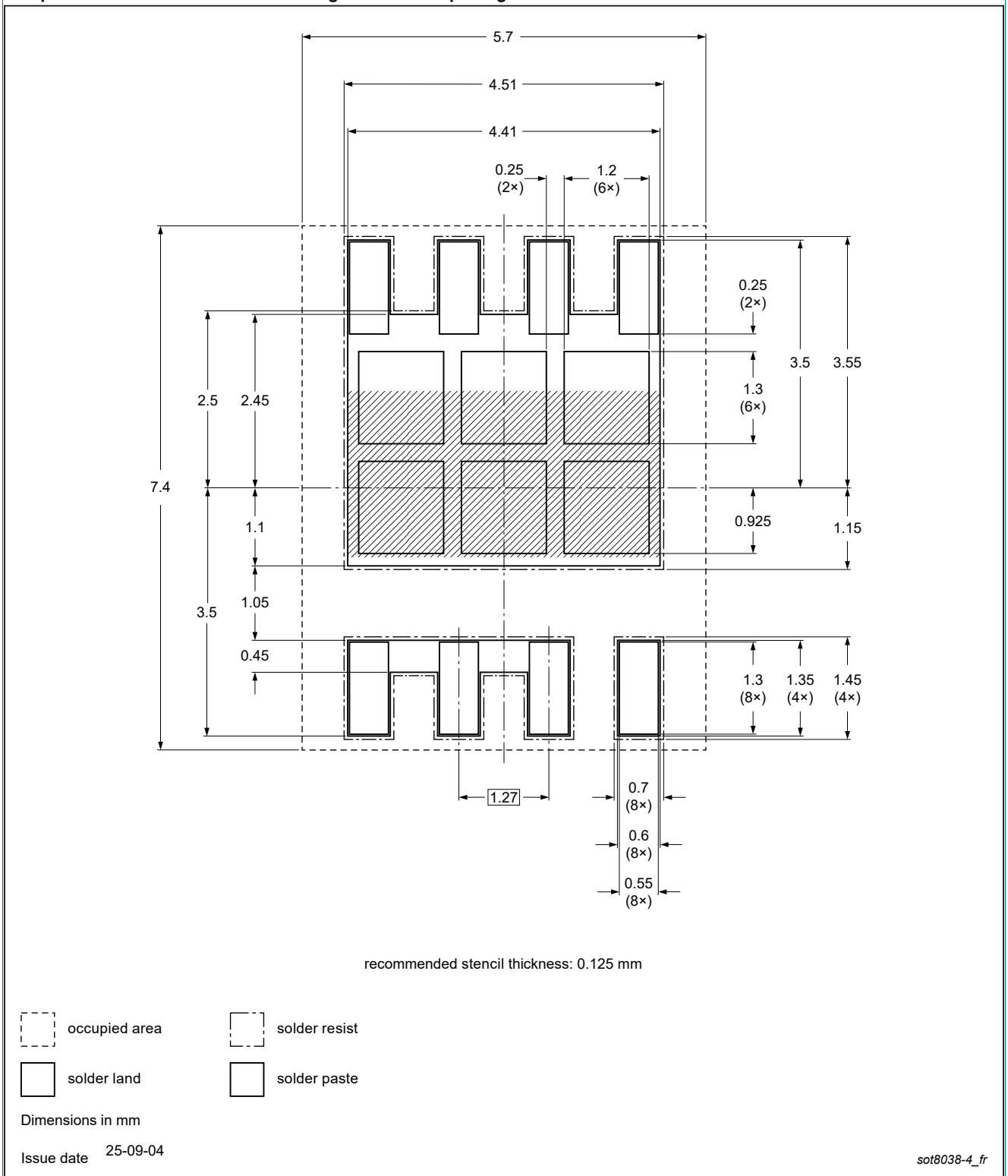


Fig. 19. Reflow Soldering Footprint for MLPAK56 (SOT8038-4)

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13. Revision History

Table 9. Revision History

Document ID	Release Date	Data Sheet Status	Supersedes
PSMNS6R5-40MYX8 V. 1	20261021	Product data sheet	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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