



PBL6002D

60 V, 1 A PNP/NPN loadswitch double transistor

1 October 2025

Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} (BISS) transistor and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

4. Quick reference data

Table 1. Quick reference data

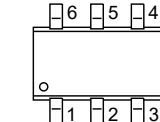
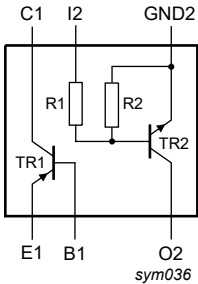
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	-60	V
I_C	collector current		[1]	-	-	-1	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1000$ mA; $I_B = -100$ mA; $T_{amb} = 25$ °C	[2]	-	255	340	mΩ
TR2; NPN resistor-equipped transistor							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)			3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	

[1] Device mounted on a ceramic PCB, Al_2O_3 , standard footprint.

[2] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 TSOP6 (SOT457)	 sym036
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS6002D	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PBLS6002D	F2

8. Limiting values

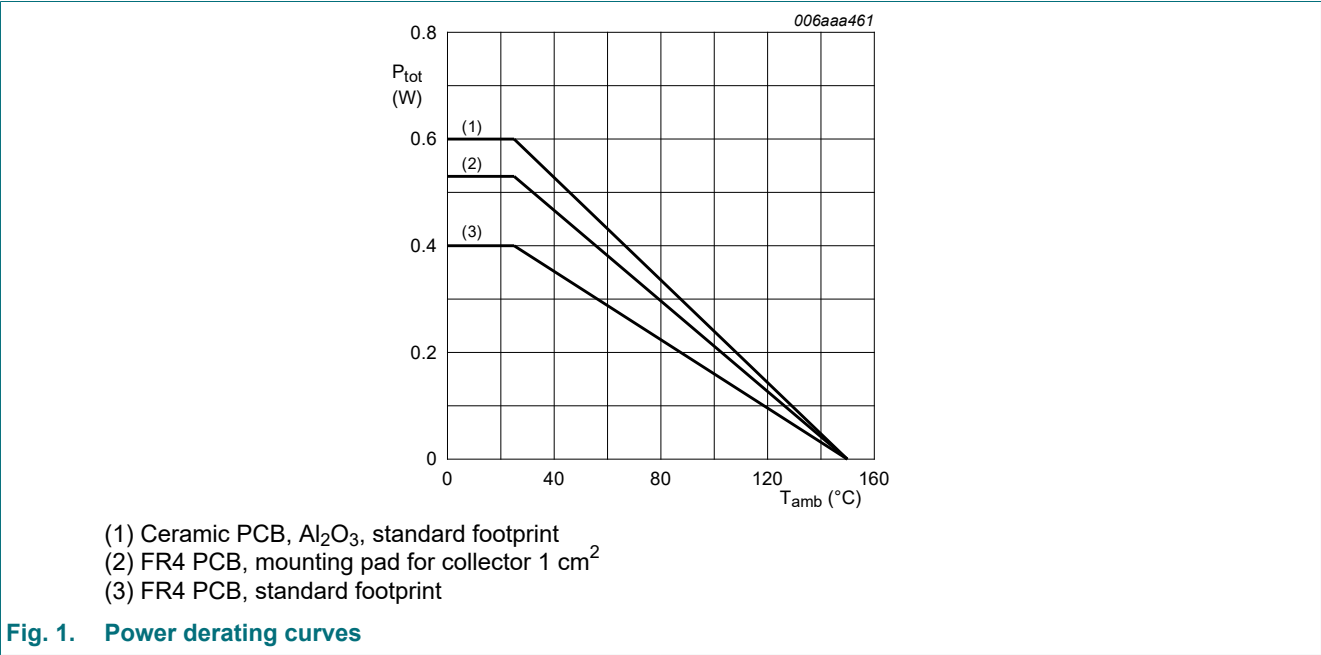
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter		-	-80	V
V_{CEO}	collector-emitter voltage	open base		-	-60	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
I_C	collector current		[1]	-	-700	mA
			[2]	-	-850	mA
			[3]	-	-1	A
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse		-	-2	A
I_B	base current			-	-300	mA
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	-1000	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW

Symbol	Parameter	Conditions		Min	Max	Unit
TR2; NPN resistor-equipped transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	30	V
I _O	output current			-	100	mA
I _{CM}	peak collector current			-	100	mA
P _{tot}	total power dissipation		[1]	-	200	mW
			[2]	-	200	mW
			[3]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	400	mW
			[2]	-	530	mW
			[3]	-	600	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	312	K/W
			[2]	-	-	236	K/W
			[3]	-	-	208	K/W
TR1; PNP low V _{CEsat} transistor							
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	105	K/W

- [1] Device mounted on an FR4 PCB, single-sided, copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

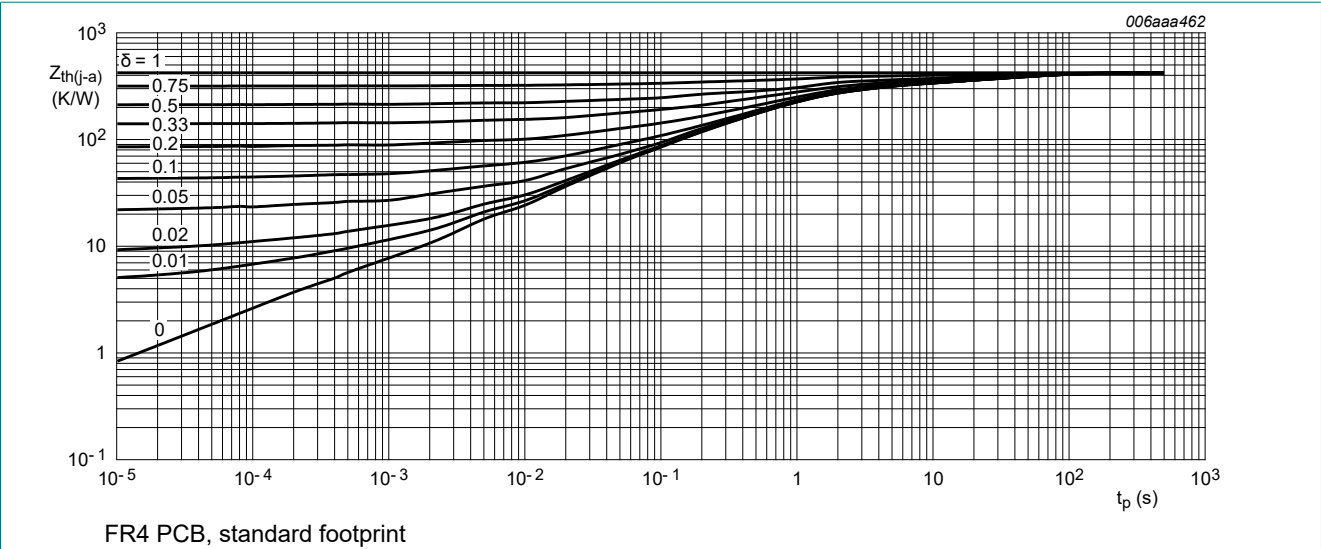


Fig. 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

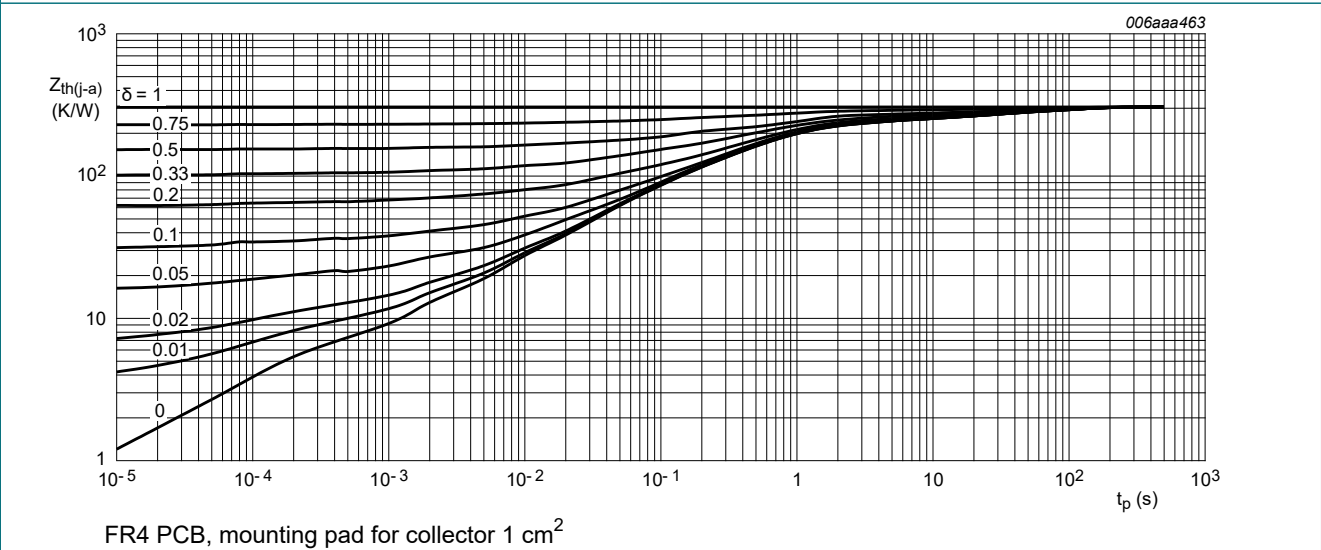


Fig. 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

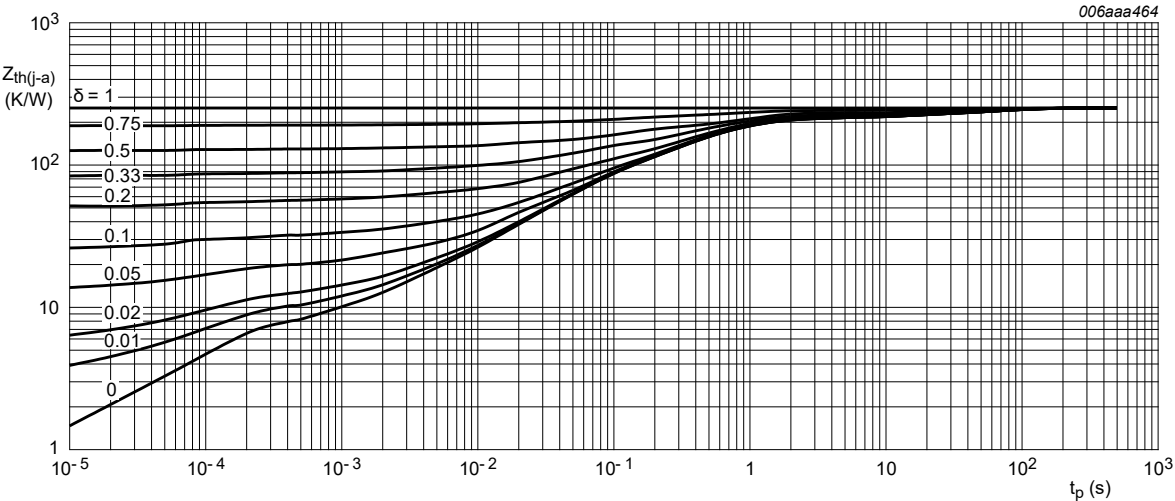


Fig. 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

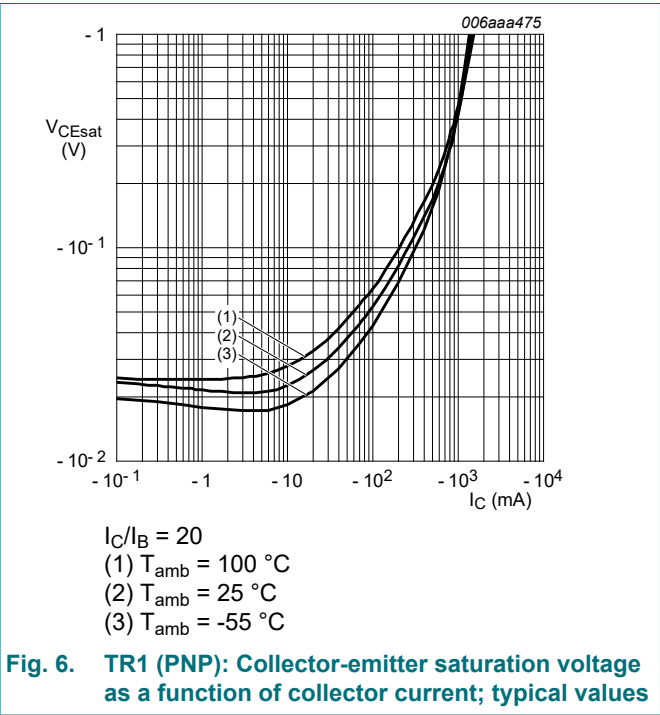
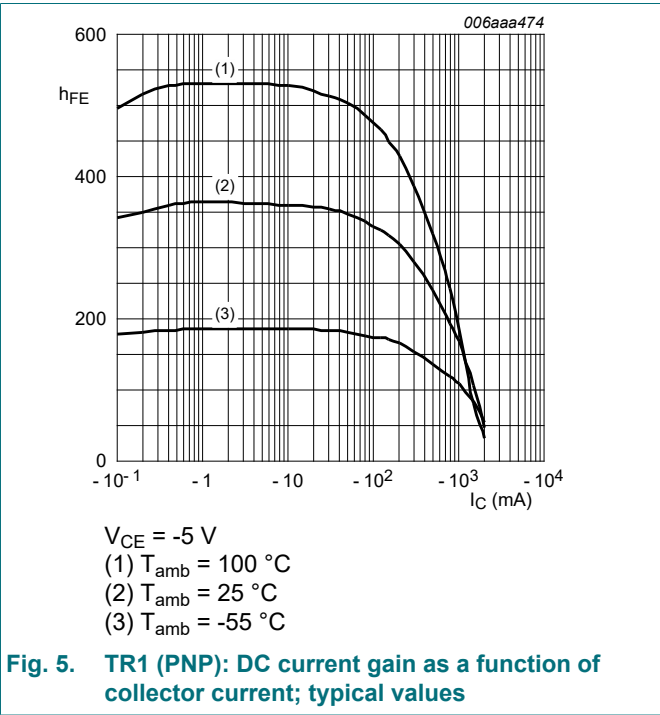
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low VCEsat transistor							
ICBO	collector-base cut-off current	V _{CB} = -60 V; I _E = 0 A; T _{amb} = 25 °C		-	-	-100	nA
		V _{CB} = -60 V; I _E = 0 A; T _j = 150 °C		-	-	-50	μA
ICES	collector-emitter cut-off current	V _{CE} = -60 V; V _{BE} = 0 V; T _{amb} = 25 °C		-	-	-100	nA
IEBO	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	-100	nA
hFE	DC current gain	V _{CE} = -5 V; I _C = -1 mA; T _{amb} = 25 °C		200	350	-	
		V _{CE} = -5 V; I _C = -500 mA; T _{amb} = 25 °C	[1]	150	230	-	
		V _{CE} = -5 V; I _C = -1000 mA; T _{amb} = 25 °C	[1]	100	160	-	
VCEsat	collector-emitter saturation voltage	I _C = -100 mA; I _B = -1 mA; T _{amb} = 25 °C		-	-110	-175	mV
		I _C = -500 mA; I _B = -50 mA; T _{amb} = 25 °C	[1]	-	-135	-180	mV
		I _C = -1000 mA; I _B = -100 mA; T _{amb} = 25 °C	[1]	-	-255	-340	mV
RCEsat	collector-emitter saturation resistance	T _{amb} = 25 °C	[1]	-	255	340	mΩ
VBEsat	base-emitter saturation voltage	I _C = -1000 mA; I _B = -50 mA; T _{amb} = 25 °C	[1]	-	-0.95	-1.1	V
VBEon	base-emitter turn-on voltage	V _{CE} = -5 V; I _C = -1000 mA; T _{amb} = 25 °C	[1]	-	-0.82	-0.9	V
td	delay time	I _C = -0.5 A; I _{Bon} = -25 mA; I _{Boff} = 25 mA; T _{amb} = 25 °C		-	11	-	ns
tr	rise time			-	30	-	ns
ton	turn-on time			-	41	-	ns
ts	storage time			-	205	-	ns
tf	fall time			-	55	-	ns
toff	turn-off time	I _C = -0.5 A; I _{Bon} = 25 mA; I _{Boff} = 25 A; T _{amb} = 25 °C		-	260	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	9	15	pF
f _T	transition frequency	V _{CE} = -10 V; I _C = -50 mA; f = 100 MHz; T _{amb} = 25 °C	150	185	-	MHz
TR2; NPN resistor-equipped transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C	-	-	1	μA
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	-	-	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	900	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 20 mA; T _{amb} = 25 °C	30	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA; T _{amb} = 25 °C	[1]	-	150	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C	-	1.1	0.5	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 20 mA; T _{amb} = 25 °C	2.5	1.9	-	V
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	-	2.5	pF

[1] Pulse test: t_p ≤ 300 μs; δ ≤ 0.02



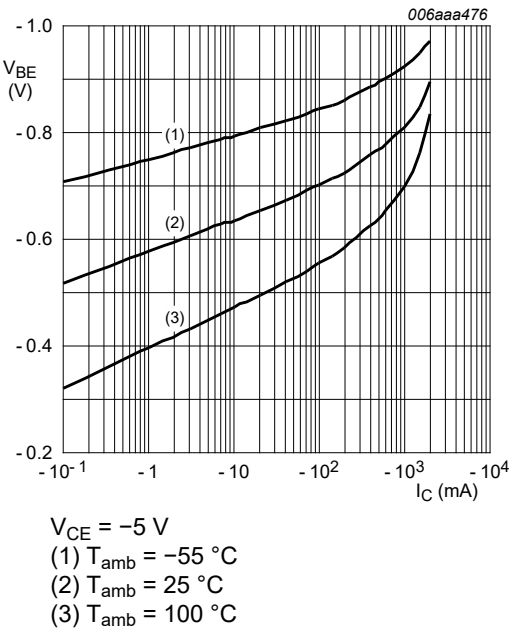


Fig. 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values

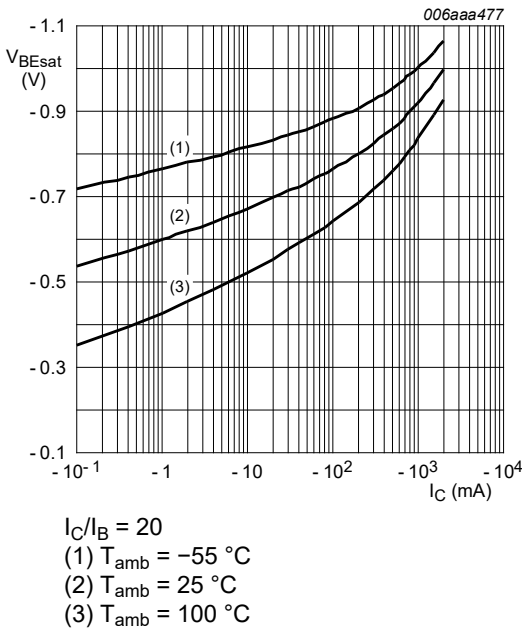


Fig. 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

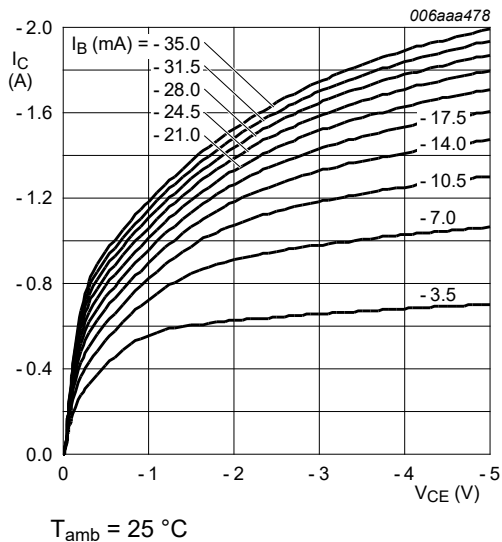


Fig. 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

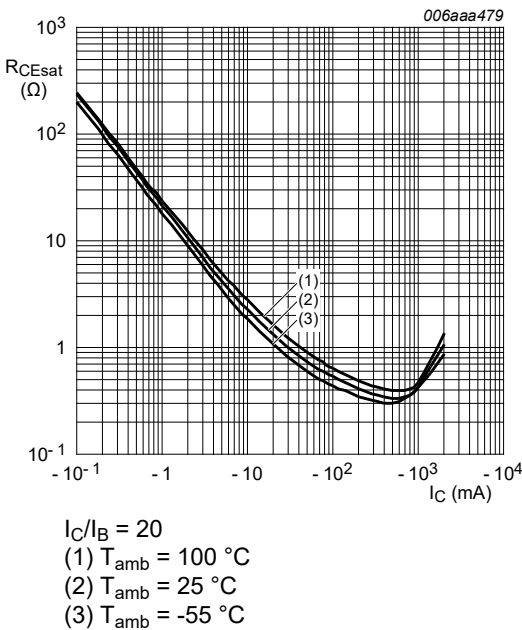


Fig. 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

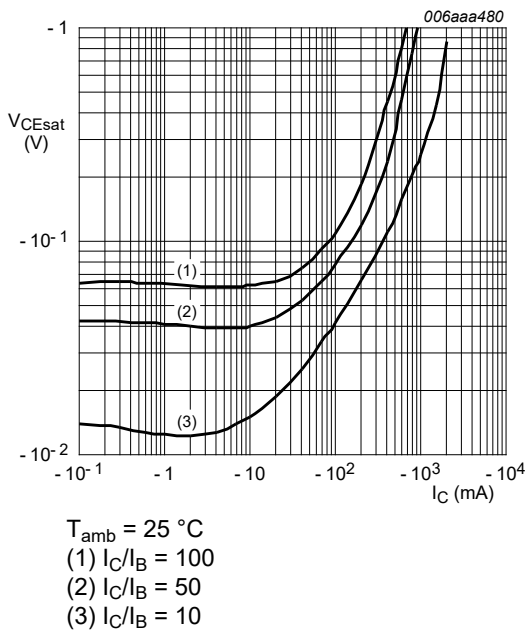


Fig. 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

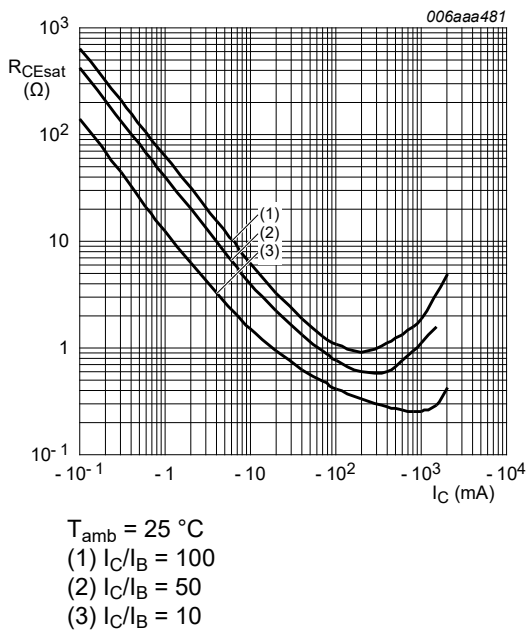


Fig. 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

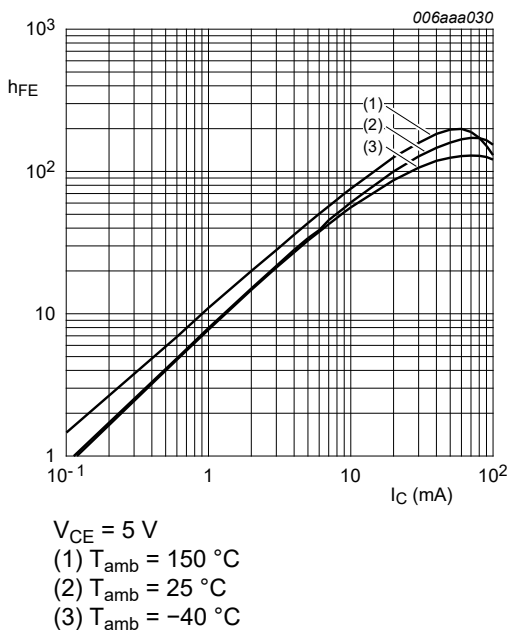


Fig. 13. TR2 (NPN): DC current gain as a function of collector current; typical values

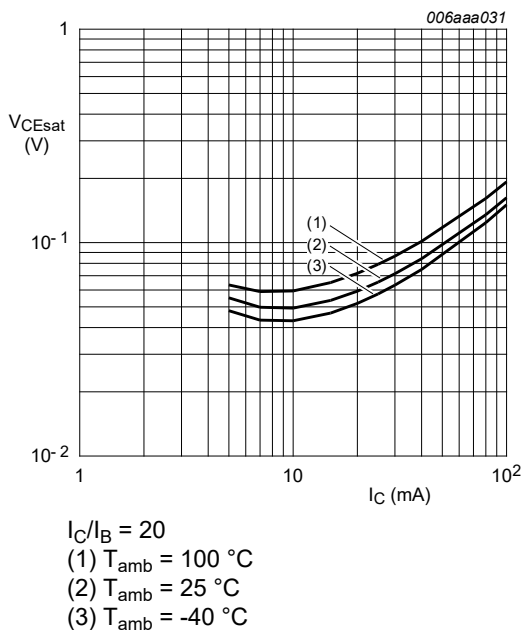


Fig. 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

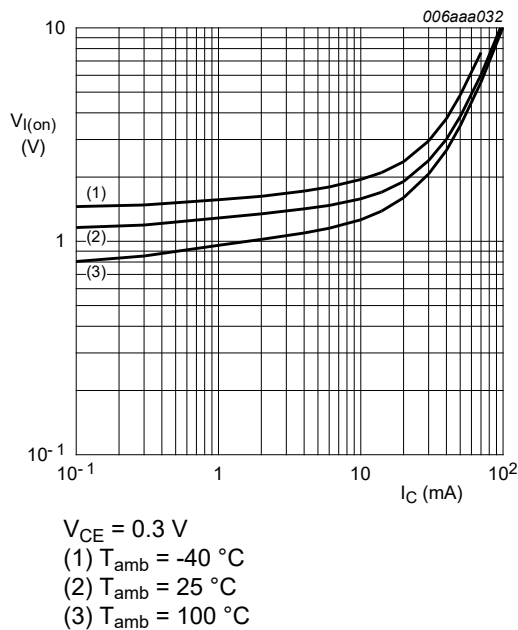


Fig. 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values

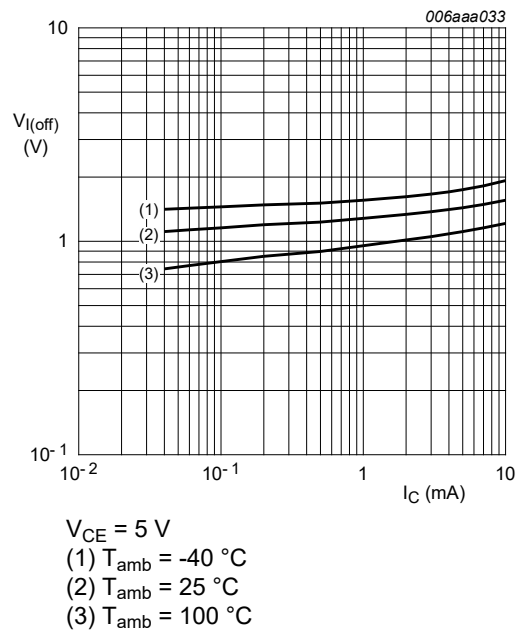


Fig. 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

11. Test information

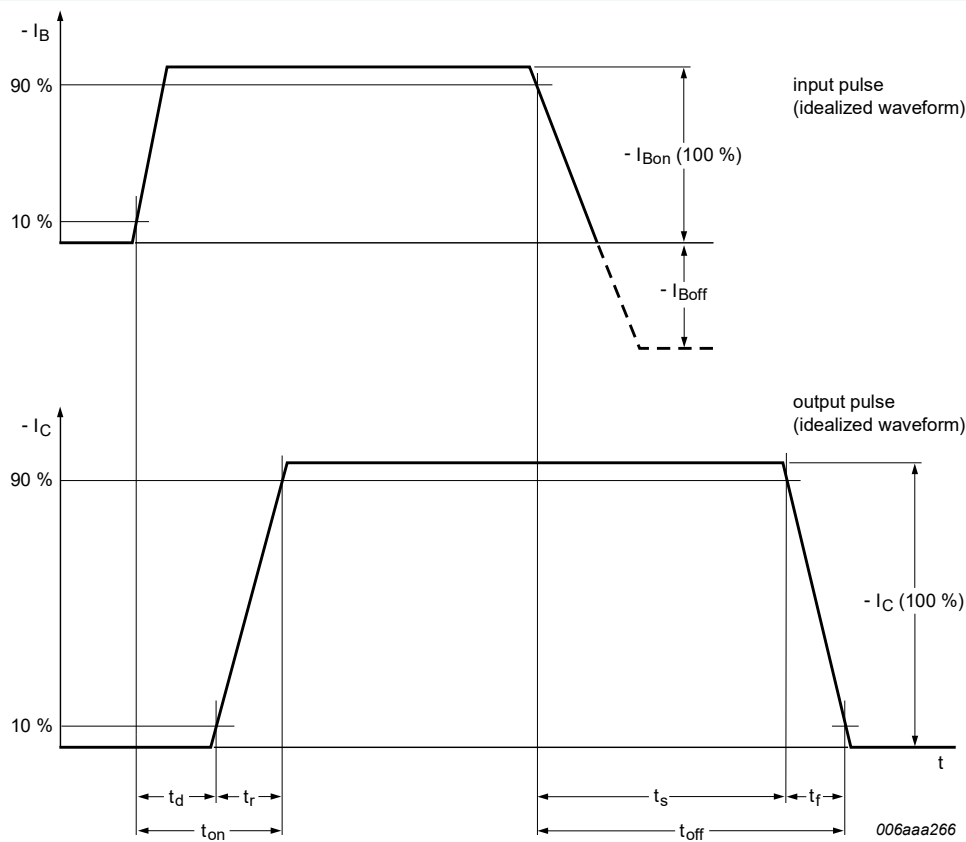
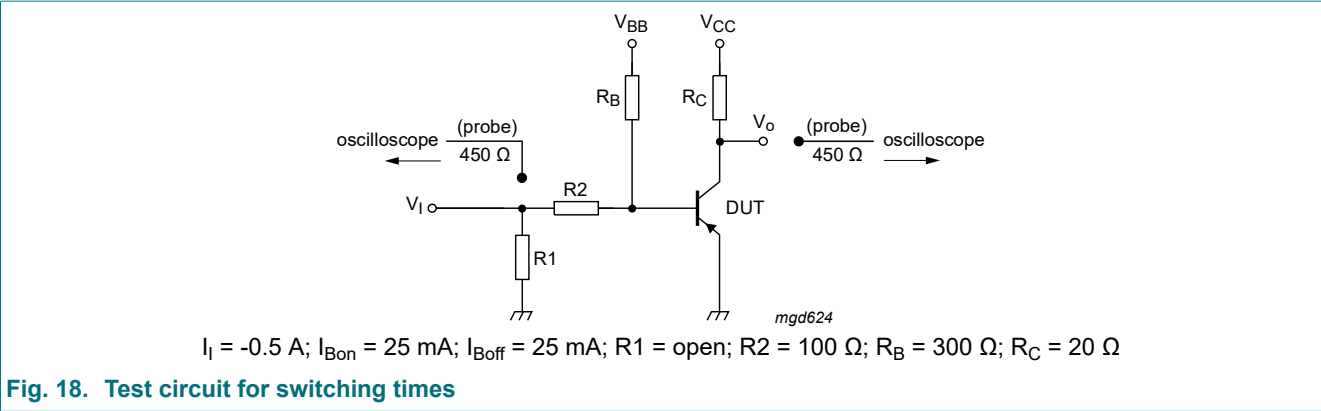
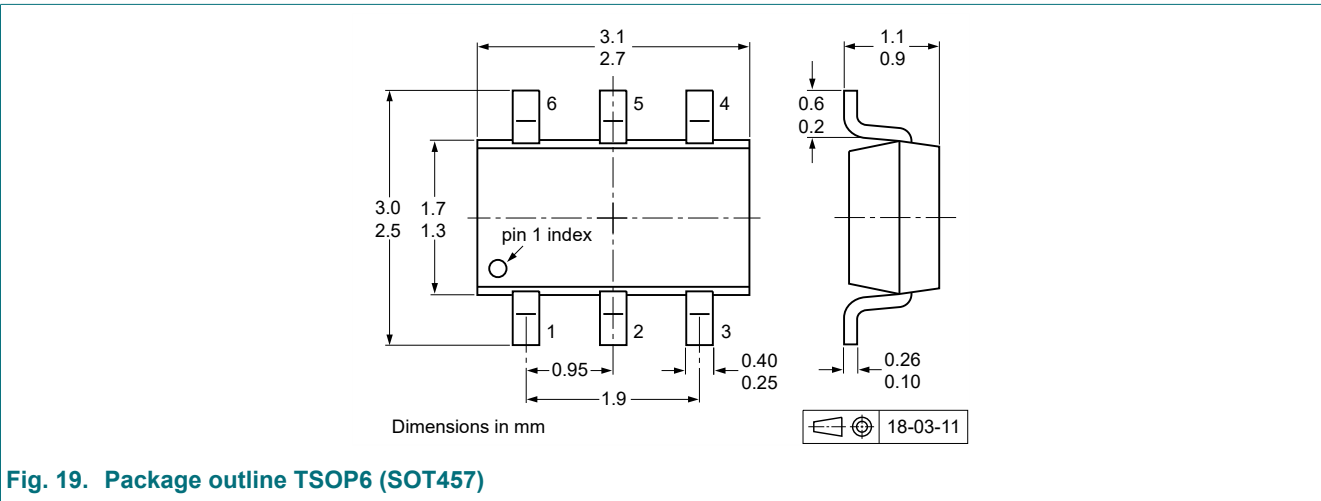


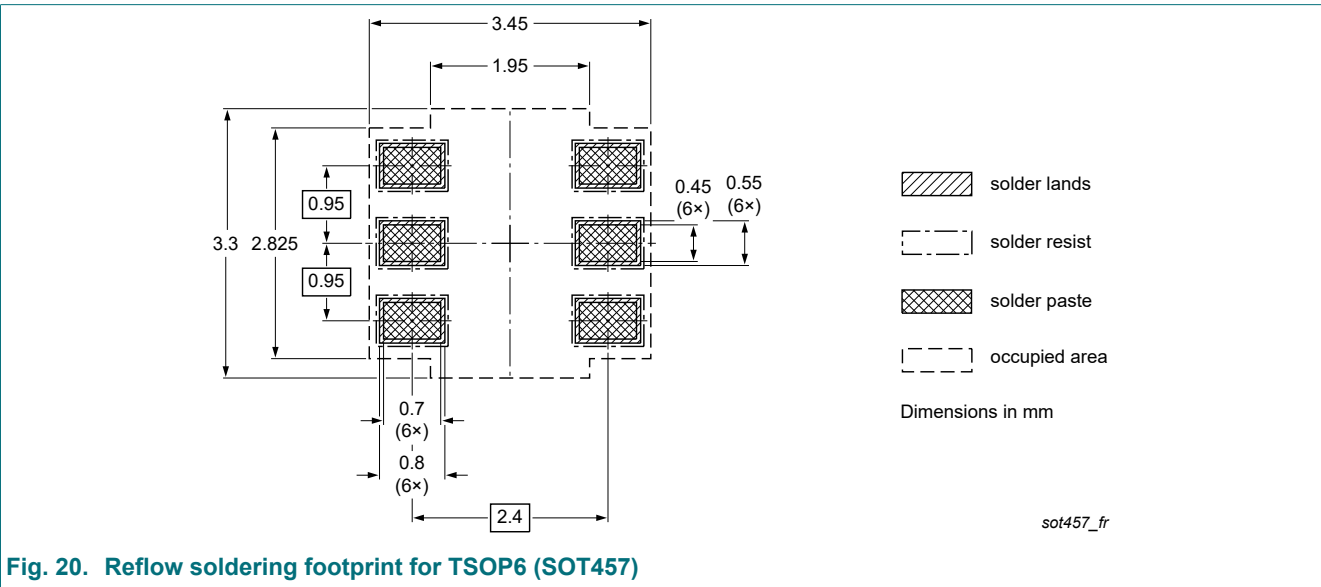
Fig. 17. Transistor switching time definition



12. Package outline



13. Soldering



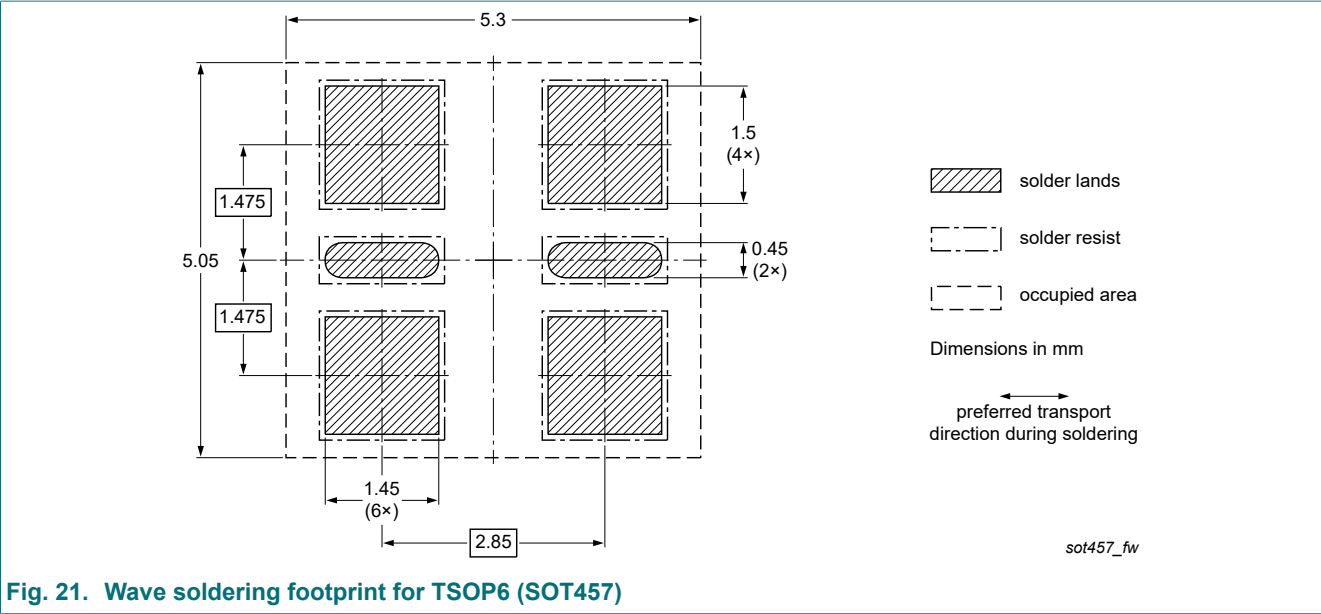


Fig. 21. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS6002D v.4	20251001	Product data sheet	-	PBLS6002D v.3
Modifications:	Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).			
PBLS6002D v.3	20231026	Product data sheet	-	PBLS6002D_2
PBLS6002D_2	20090907	Product data sheet	-	PBLS6002D_1
PBLS6002D_1	20050623	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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