NS50T07Y1M7

650 V, 50 A Three-phase Full-bridge IGBT Power Module

Rev. 1 — 8 July 2026 Product data sheet

1. General Description

The NS50T07Y1M7 is an insulated-gate bipolar transistor (IGBT) power module. The module uses 7th-generation carrier stored trench-gate and field-stop (FS) technology. It is designed for high-voltage industrial applications, including power inverters and motor drives.

2. Features

- Three-phase full-bridge topology with an NTC temperature sensor
- Rated voltage and current: 650 V/50 A
- Maximum junction temperature: 175 °C
- Short-circuit withstand time: 5 µs
- Solderable auxiliary contacts
- Optimized design for low parasitic inductance
- Low collector-emitter saturation voltage
- Low switching losses
- Validated with enhanced 2,000-hour HTRB and HV-H3TRB qualification testing

3. Applications

- Motor drives
- Servo drives
- Air conditioning systems
- Renewable energy systems
- Uninterruptible power supply (UPS) inverters

4. Quick Reference Data

Table 1. Quick Reference Data

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CES}	collector-emitter voltage	T_{vj} = 25 °C	-	650	V
I_{CDC}	continuous DC collector current	T_c = 90 °C	-	56	A
		T_c = 100 °C	-	51	A
$T_{vj(op)}$	operating junction temperature		−40	175	°C

Fig. 1. Product Outline

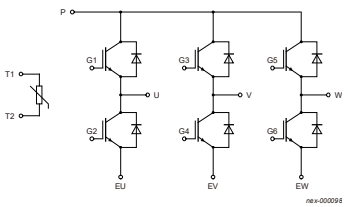


Fig. 2. Topology

5. Characteristic

5.1. IGBT

Table 2. Maximum Limiting Values

All values at T_{vj} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CES}	collector-emitter voltage		-	650	V
I_{CDC}	continuous DC collector current[1]	T_c = 90 °C	-	56	A
		T_c = 100 °C	-	51	A
I_{CRM}	repetitive peak collector current[2]		-	100	A
V_{GE}	gate-emitter voltage		−20	20	V
$T_{vj(op)}$	operating junction temperature		−40	175	°C

[1] Value is given at chip level, and is limited by $T_{vj(max)}$.
[2] Time duration is limited by $T_{vj(max)}$.

Table 3. Electrical Characteristics

All values at T_{vj} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
$V_{CE(sat)}$	collector-emitter saturation voltage[1]	V_{GE} = 15 V; I_C = 50 A	-	1.32	1.62	V
		V_{GE} = 15 V; I_C = 50 A; T_{vj} = 125 °C	-	1.48	-	V
		V_{GE} = 15 V; I_C = 50 A; T_{vj} = 175 °C	-	1.56	-	V
$V_{GE(th)}$	gate-emitter threshold voltage	I_C = 0.5 mA; V_{CE} = V_{GE}	4.35	5.0	5.65	V
I_{CES}	zero gate voltage collector current	V_{CE} = 650 V; V_{GE} = 0 V	-	-	100	µA
I_{GES}	gate-emitter leakage current	V_{CE} = 0 V; V_{GE} = 20 V	-	-	100	nA
r_g	internal gate resistor		-	0	-	Ω
C_{ies}	input capacitance	V_{CE} = 25 V; V_{GE} = 0 V; f = 100 kHz	-	3.11	-	nF
C_{oes}	output capacitance		-	0.17	-	nF
C_{res}	reverse transfer capacitance		-	0.04	-	nF
Q_G	gate charge	V_{CC} = 400 V; I_C = 50 A; V_{GE} = 15 V	-	0.49	-	µC

[1] Value is given at chip level.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Switching Characteristics							
$t_{d(on)}$	turn-on delay time	V_{GE} = ± 15 V; V_{CC} = 400 V; I_C = 50 A; $R_{G(on)}$ = 5.0 Ω $R_{G(off)}$ = 36 Ω; di/dt = 1590 A/µs (only at turn-on, T_{vj} = 175 °C) dv/dt = 3690 V/µs (only at turn-off, T_{vj} = 175 °C)	T_{vj} = 25 °C	-	23	-	ns
			T_{vj} = 125 °C	-	26	-	ns
			T_{vj} = 175 °C	-	27	-	ns
t_r	rise time		T_{vj} = 25 °C	-	23	-	ns
			T_{vj} = 125 °C	-	26	-	ns
			T_{vj} = 175 °C	-	28	-	ns
$t_{d(off)}$	turn-off delay time		T_{vj} = 25 °C	-	444	-	ns
			T_{vj} = 125 °C	-	474	-	ns
			T_{vj} = 175 °C	-	494	-	ns
t_f	fall time		T_{vj} = 25 °C	-	23	-	ns
			T_{vj} = 125 °C	-	23	-	ns
			T_{vj} = 175 °C	-	26	-	ns
E_{on}	turn-on switching energy loss		T_{vj} = 25 °C	-	958	-	µJ
			T_{vj} = 125 °C	-	1296	-	µJ
			T_{vj} = 175 °C	-	1430	-	µJ
E_{off}	turn-off switching energy loss		T_{vj} = 25 °C	-	1248	-	µJ
			T_{vj} = 125 °C	-	1464	-	µJ
			T_{vj} = 175 °C	-	1585	-	µJ
$I_{C(sc)}$	short-circuit current[1]	V_{GE} = ±15 V; V_{CEmax} = V_{CES} - L_{sCE} * di/dt	V_{CC} = 330 V; t_p ≤ 5 µs; T_{vj} = 100 °C	-	266	-	A
			V_{CC} = 400 V; t_p ≤ 3 µs; T_{vj} = 150 °C	-	251	-	A
Thermal Resistance							
$R_{th(j-c)}$	thermal resistance from junction to case	per IGBT switch		-	-	0.752	K/W
$R_{th(c-h)}$	thermal resistance from case to heatsink	per IGBT switch; λ_{grease} = 3 W/(m·K)		-	0.577	-	K/W

[1] Short-circuit cycles ≤ 1000. Time between tests ≥ 10 s.

5.2. Diode

Table 4. Maximum Limiting Values

All values at T_{vj} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	650	V
I_F	continuous DC forward current[1]		-	50	A
I_{FRM}	repetitive peak forward current[2]		-	100	A
I^2t	I^2t value	V_R = 0 V; t_P = 10 ms; T_{vj} = 175 °C	-	134	A^2s
$T_{vj(op)}$	operating junction temperature		−40	175	°C

[1] Value is given at chip level.
[2] Time duration is limited by $T_{vj(max)}$.

Table 5. Electrical Characteristics

All values at T_{vj} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	diode forward voltage[1]	V_{GE} = 0 V; I_F = 50 A	T_{vj} = 25 °C	-	1.69	2.04	V
			T_{vj} = 125 °C	-	1.63	-	V
			T_{vj} = 175 °C	-	1.58	-	V
t_{rr}	reverse recovery time	V_R = 400 V; I_F = 50 A; di_F/dt = 1590 A/µs (only at T_{vj} = 175 °C)	T_{vj} = 25 °C	-	52	-	ns
			T_{vj} = 125 °C	-	76	-	ns
			T_{vj} = 175 °C	-	89	-	ns
Q_{rr}	reverse recovery charge		T_{vj} = 25 °C	-	1.39	-	µC
			T_{vj} = 125 °C	-	2.38	-	µC
			T_{vj} = 175 °C	-	3.06	-	µC
I_{rrm}	peak reverse recovery current		T_{vj} = 25 °C	-	49	-	A
			T_{vj} = 125 °C	-	61	-	A
			T_{vj} = 175 °C	-	68	-	A
E_{rec}	reverse recovery energy loss		T_{vj} = 25 °C	-	382	-	µJ
			T_{vj} = 125 °C	-	700	-	µJ
			T_{vj} = 175 °C	-	870	-	µJ
$R_{th(j-c)}$	thermal resistance from junction to case	per diode switch		-	-	1.095	K/W
$R_{th(c-h)}$	thermal resistance from case to heatsink	per diode switch; λ_{grease} = 3 W/(m·K)		-	0.701	-	K/W

[1] Value is given at chip level.

5.3. NTC Thermistor

Table 6. NTC Thermistor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{25}	rated resistance	T_{NTC} = 25 °C	-	5	-	kΩ
ΔR/R	deviation of R_{100}	T_{NTC} = 100 °C; R_{100} = 491	−5.5	-	5.5	%
P_{25}	power dissipation	T_{NTC} = 25 °C	-	-	20	mW
$B_{25/50}$	B-value		-	3375	-	K
$B_{25/80}$	B-value		-	3425	-	K
$B_{25/100}$	B-value		-	3443	-	K

5.4. Package

Table 7. Mechanical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RTI	relative thermal index (electrical)	housing only	-	130	-	°C
L_{sCE}	internal stray inductance		-	20	-	nH
$R_{CC'+EE'}$	lead resistance, terminal to chip	T_c = 25 °C, per switch	-	4.4	-	mΩ
G	weight		-	22	-	g
T_{stg}	storage temperature		-40	-	125	°C
F	mounting force per clamp		20	-	50	N

Table 8. Insulation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISOL}	isolation test voltage	RMS; f = 50 Hz; t = 1 min	-	2.5	-	kV
	material of substrate isolation		-	Al_2O_3	-	-
	creepage distance	terminal to heatsink	-	14	-	mm
		terminal to terminal	-	6.5	-	mm
	clearance distance	terminal to heatsink	-	10.0	-	mm
		terminal to terminal	-	5.2	-	mm
CTI	comparative tracking index		200	-	-	

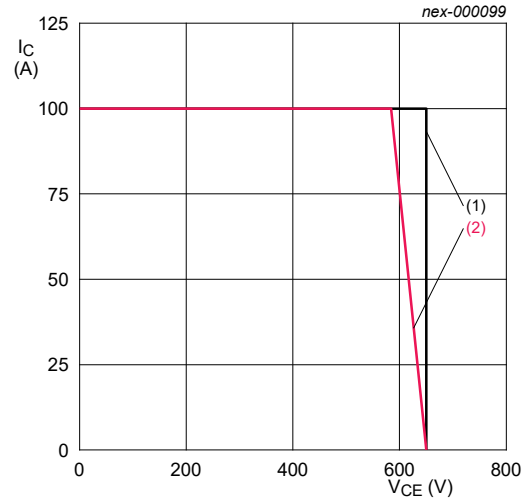
6. Ordering Information

Table 9. Ordering information

Type number	Package		
	Name	Description	Version
NS50T07Y1M7	NY1	IGBT power module with three-phase full-bridge circuit topology; Solderable auxiliary contacts; Outline dimension 62.8 mm × 33.8 mm × 15.5 mm	SOT8130-2

7. Characteristic Diagram

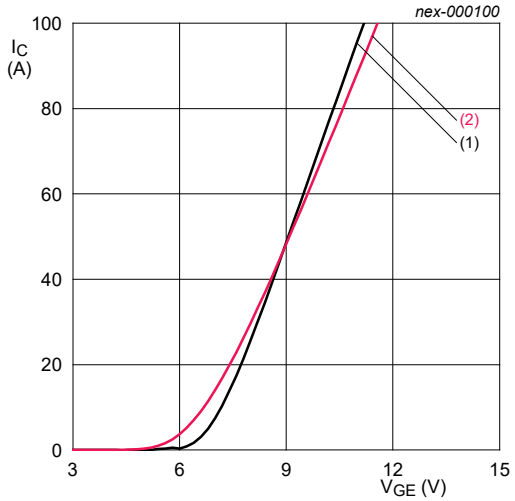
Table 10. Waveforms and Output Characteristics



V_{GE} = ± 15 V; $R_{G(off)}$ = 36 Ω; T_{vj} = 175 °C

- (1) Chip
- (2) Module

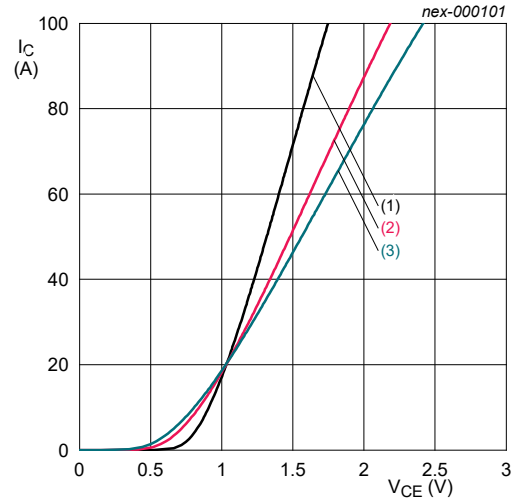
Fig. 3. Reverse Bias Safe Operation Area



V_{CE} = 20 V

- (1) T_{vj} = 25 °C
- (2) T_{vj} = 175 °C

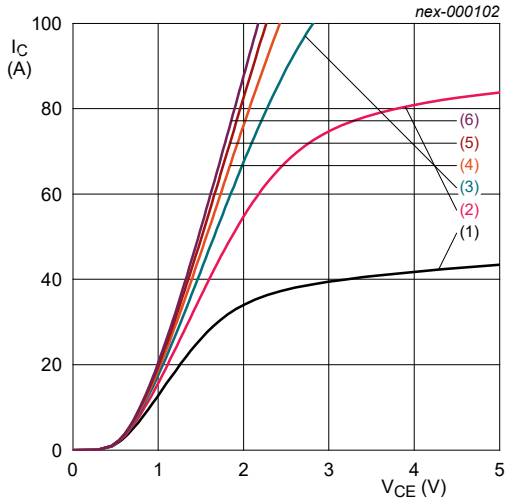
Fig. 4. Collector Current as a Function of Gate-emitter Voltage



V_{GE} = 15 V

- (1) T_{vj} = 25 °C
- (2) T_{vj} = 125 °C
- (3) T_{vj} = 175 °C

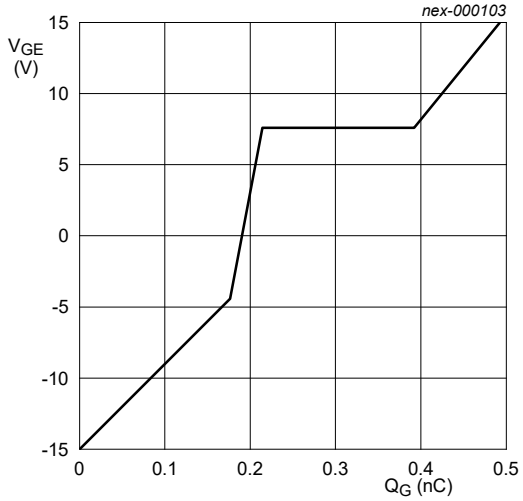
Fig. 5. Collector Current as a Function of Collector-emitter Voltage, Chip Level



T_{vj} = 175 °C

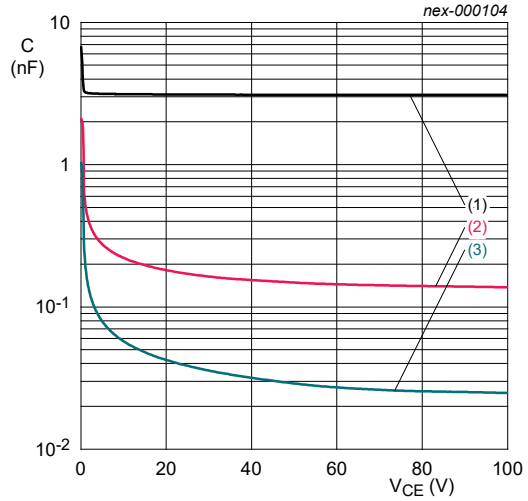
- (1) V_{GE} = 9 V
- (2) V_{GE} = 11 V
- (3) V_{GE} = 13 V
- (4) V_{GE} = 15 V
- (5) V_{GE} = 17 V
- (6) V_{GE} = 19 V

Fig. 6. Collector Current as a Function of Collector-emitter Voltage, Chip Level



I_C = 50 A; V_{CE} = 400 V

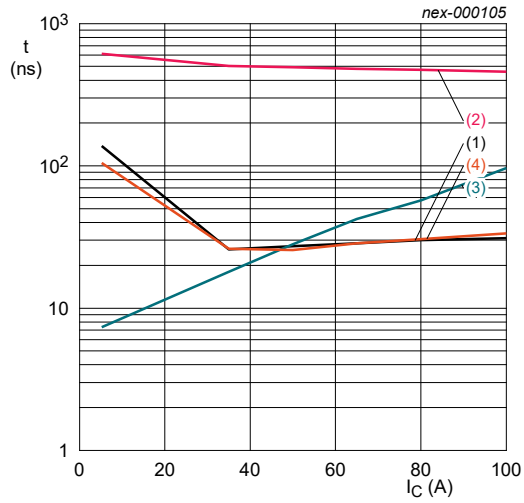
Fig. 7. Gate-emitter Voltage as a Function of Gate Charge



V_{GE} = 0 V; f = 100 kHz

- (1) C_{ies}
- (2) C_{oes}
- (3) C_{res}

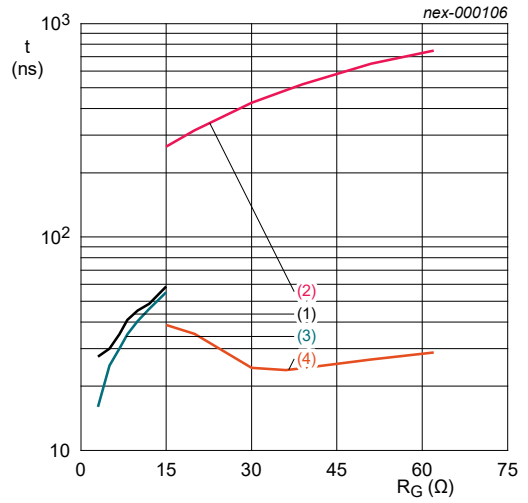
Fig. 8. Typical Capacitance as a Function of Collector-emitter Voltage



V_{GE} = ± 15 V; V_{CC} = 400 V; T_{vj} = 175 °C; $R_{G(on)}$ = 5 Ω; $R_{G(off)}$ = 36 Ω

- (1) $t_{d(on)}$
- (2) $t_{d(off)}$
- (3) t_r
- (4) t_f

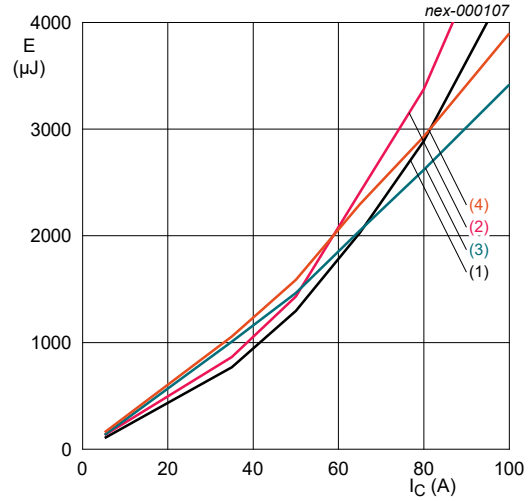
Fig. 9. Typical Switching Times as a Function of Collector Current



V_{GE} = ± 15 V; V_{CC} = 400 V; I_C = 50 A; T_{vj} = 175 °C

- (1) $t_{d(on)}$
- (2) $t_{d(off)}$
- (3) t_r
- (4) t_f

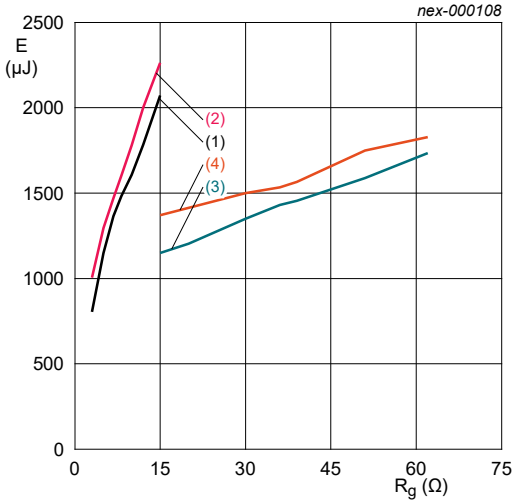
Fig. 10. Typical Switching Times as a Function of Gate Resistance



V_{GE} = ± 15 V; V_{CC} = 400 V
$R_{G(on)}$ = 5 Ω; $R_{G(off)}$ = 36 Ω

- (1) E_{on}, T_{vj} = 125 °C
- (2) E_{on}, T_{vj} = 175 °C
- (3) E_{off}, T_{vj} = 125 °C
- (4) E_{off}, T_{vj} = 175 °C

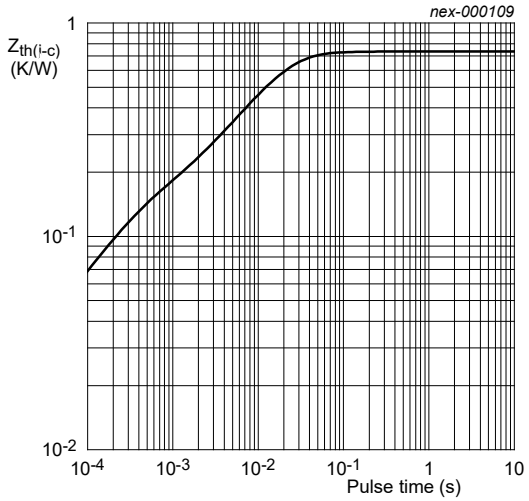
Fig. 11. Typical Switching Energy Losses as a Function of Collector Current



V_{GE} = ± 15 V; V_{CC} = 400 V; I_C = 50 A

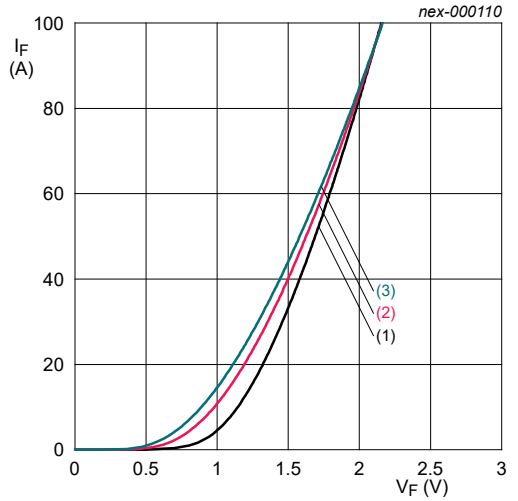
- (1) E_{on}, T_{vj} = 125 °C
- (2) E_{on}, T_{vj} = 175 °C
- (3) E_{off}, T_{vj} = 125 °C
- (4) E_{off}, T_{vj} = 175 °C

Fig. 12. Typical Switching Energy Losses as a Function of Gate Resistance



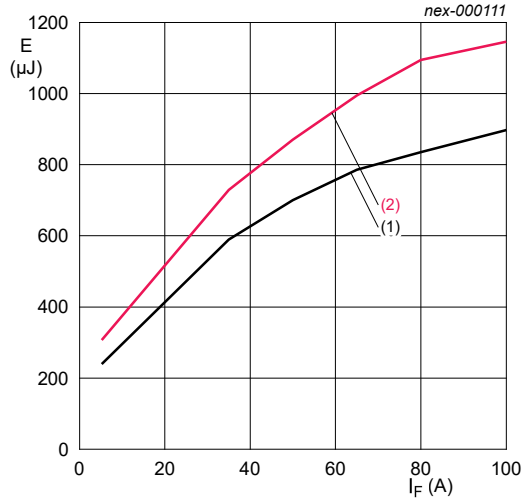
i	1	2	3	4
r_i [K/W]	0.01557	0.00760	0.11972	0.60867
τ_i [s]	0.000004	0.000029	0.000334	0.016602

Fig. 13. Transient Thermal Impedance of IGBT as a Function of Single Pulse



- (1) T_{vj} = 25 °C
- (2) T_{vj} = 125 °C
- (3) T_{vj} = 175 °C

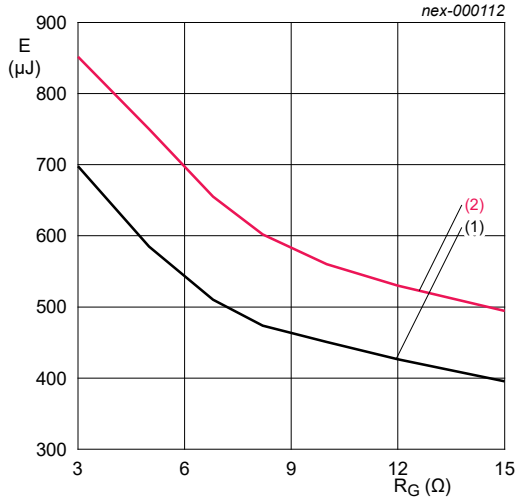
Fig. 14. Typical Diode Forward Current as a Function of Forward Voltage, Chip Level



V_R = 400 V; $R_{G(on)}$ = 5.0 Ω

- (1) T_{vj} = 125 °C
- (2) T_{vj} = 175 °C

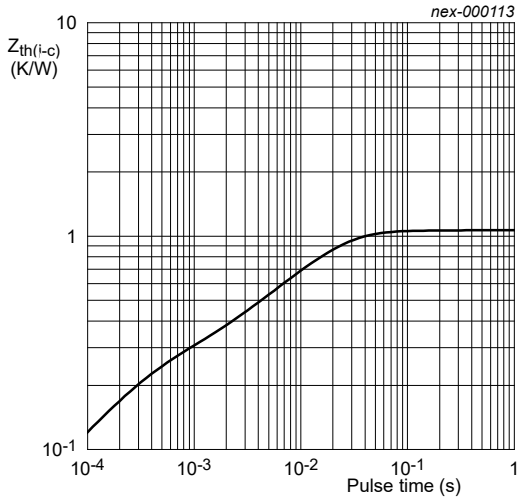
Fig. 15. Typical Reverse Recovery Energy Loss as a Function of Forward Current



V_R = 400 V; I_F = 50 A

- (1) T_{vj} = 125 °C
- (2) T_{vj} = 175 °C

Fig. 16. Typical Reverse Recovery Energy Loss as a Function of Gate Resistance



i	1	2	3	4
r_i [K/W]	0.02522	0.00946	0.22449	0.83590
τ_i [s]	0.000003	0.000023	0.000295	0.017238

Fig. 17. Transient Thermal Impedance of Diode as a Function of Single Pulse

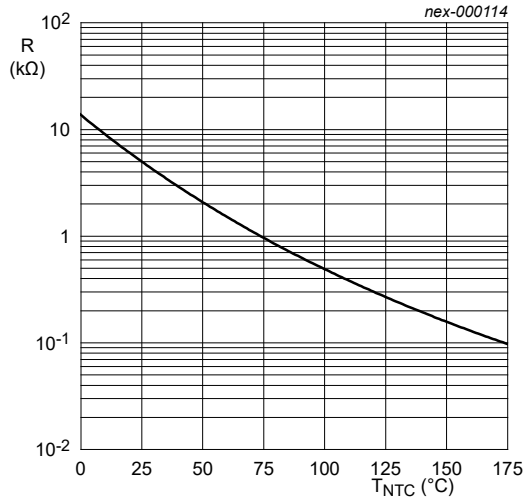


Fig. 18. NTC-thermistor Characteristics

8. Waveform Definition

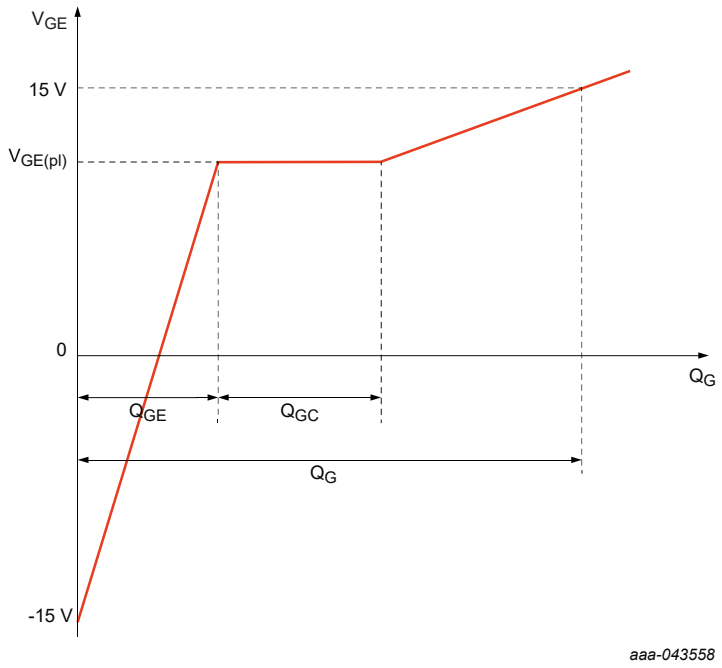
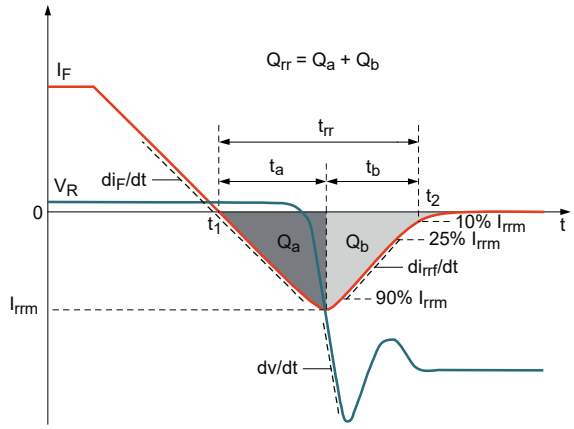


Fig. 19. IGBT Gate Charge Waveform Definitions



$$E_{rec} = \int_{t_1}^{t_2} V_R \times I_F \times dt$$

Fig. 20. Diode Reverse Recovery Waveform Definitions

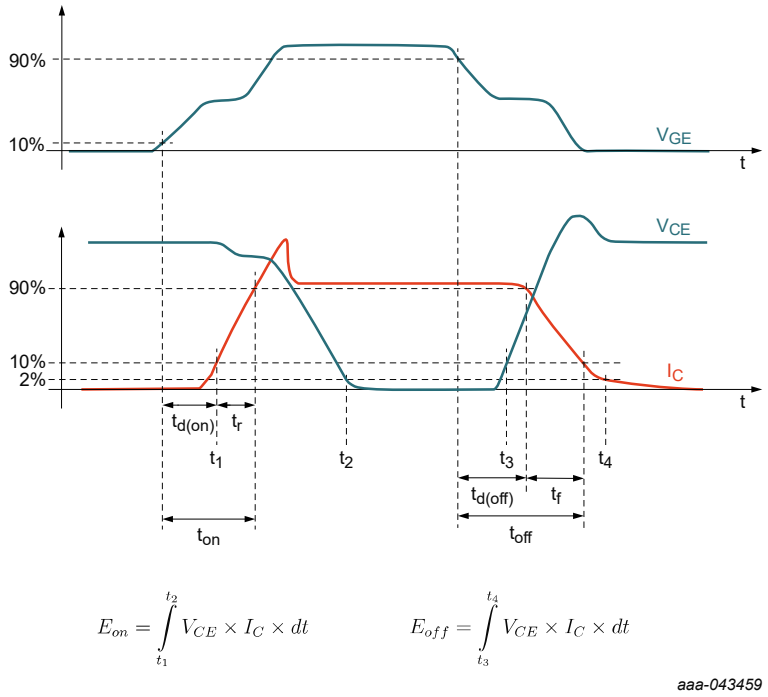


Fig. 21. IGBT Switching Times and Energy Loss Definitions

9. Circuit Diagram

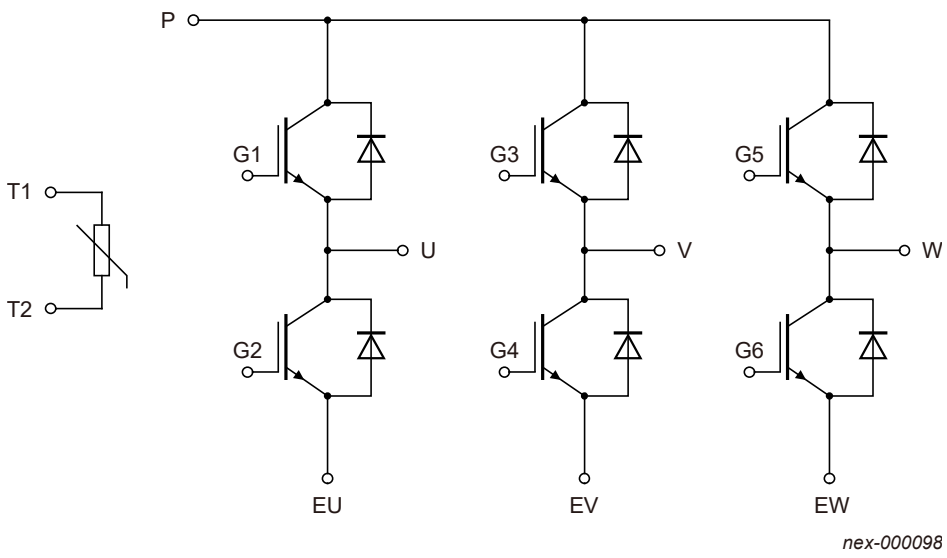


Fig. 22. Circuit Diagram

10. Package Outline

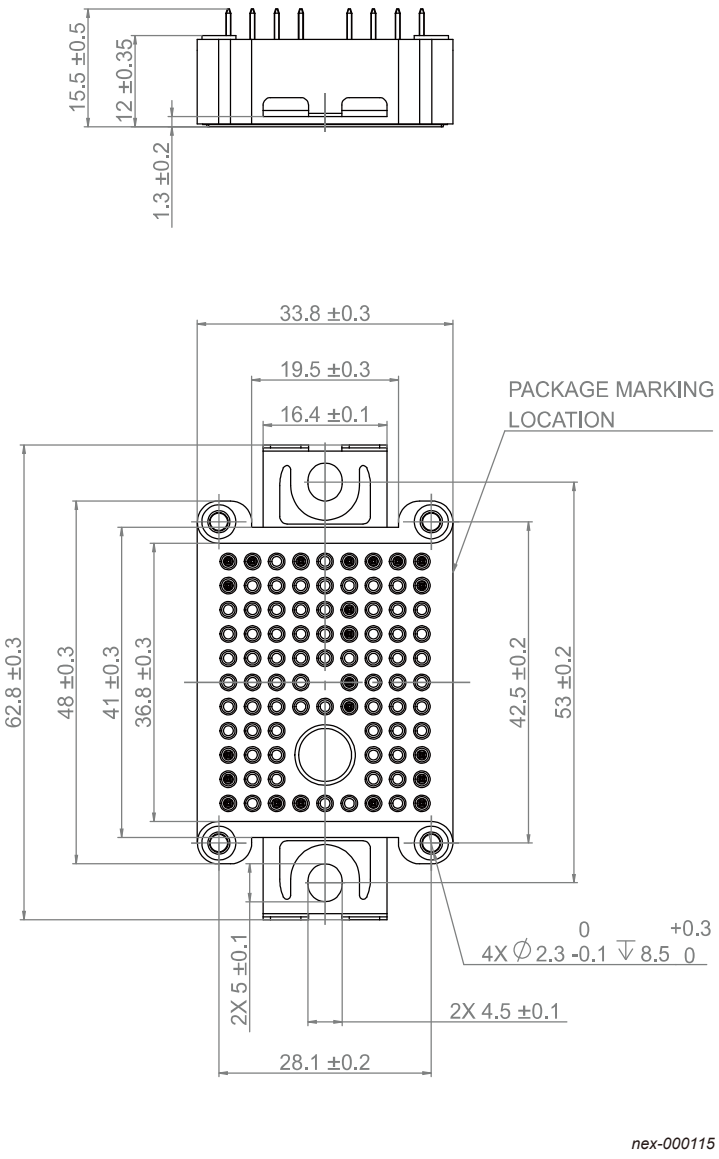


Fig. 23. Package Outline

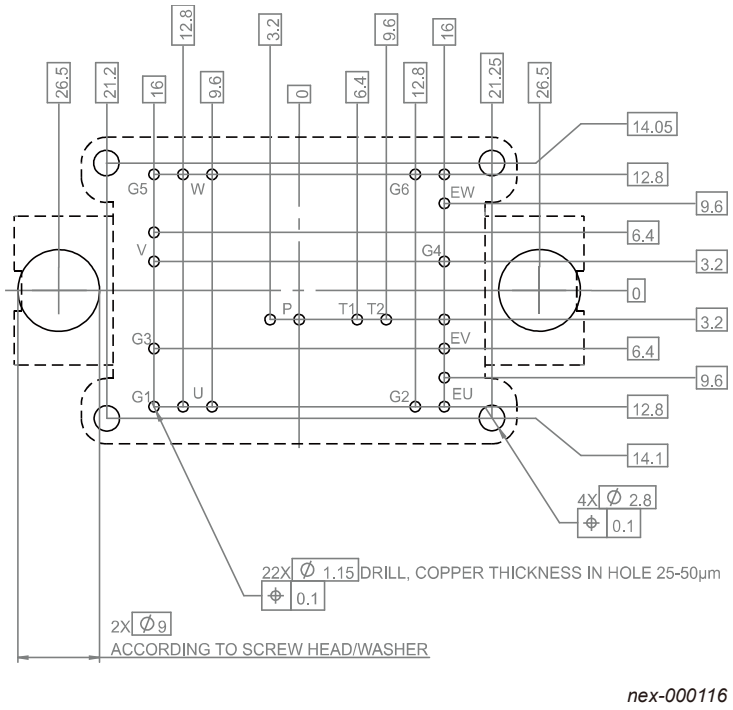


Fig. 24. PCB Hole Pattern

11. Revision History

Table 11. Revision History

Document ID	Release Date	Data Sheet Status	Supersedes
NS50T07Y1M7 v.1	20260708	Product data sheet	-

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

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