NEX81811DA; NEX81812DA

Adaptive Synchronous Rectifier (SR) Controller

Rev. 1.1 — 22 December 2025 Product data sheet

1. General description

The NEX81811DA and NEX81812DA (NEX81811/2DA) are high performance synchronous rectification controllers used in switching mode power supplies. It supports operation in Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM) and quasi-resonant flyback converters.

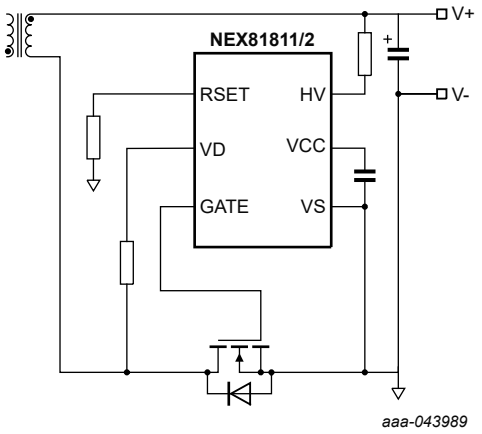
The NEX81811/2DA regulates the forward drop voltage of an external synchronous rectifier (SR) MOSFET in two stages. This allows the SR FET to turn off quickly when the V_{DS} becomes positive.

The externally adjustable turn-on blanking time can effectively prevent the synchronous rectifier from being falsely turned off due to leakage inductance and parasitic parameter oscillation.

The adaptive turn-on detection circuit can prevent the SR from being mistakenly turned on when the V_{DS} DCM oscillation crosses zero during some load conditions. The adaptive turn-on detection circuit also enhances SR conduction efficiency during light load conditions, thereby improving the average efficiency of the power supply across the entire load range.

The synchronous switch can be configured at high-side or low-side output without auxiliary windings or other power sources, because the NEX81811/2DA has a self-supply capability.

The NEX81811/2DA uses TSOT23-6 packaging with low thermal resistance. This can effectively reduce the junction temperature of the chip, making it suitable for high-density power supply design.



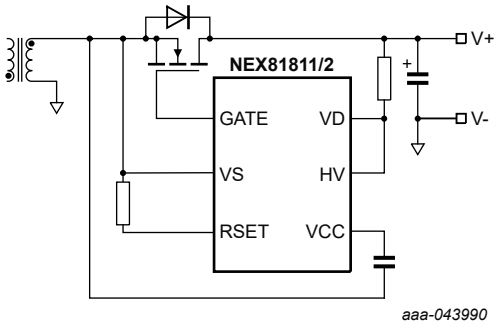
aaa-043989

2. Features and benefits

- Supports DCM, CCM, QR operation
- Supports up to 800 kHz switching frequency
- Standard and logic level MOSFET driving capability
- Wide output range down to 0 V with 2-channel VCC supply
- No need for auxiliary winding for high-side or low-side rectification
- Smart proportional gate driver for fast SR turn-off at CCM
- Adjustable turn-on blanking time for increased noise immunity
- Proprietary adaptive turn-on detection prevents SR FET from falsely turning on during DCM operation
- 10 ns typical turn-off propagation delay
- Available in a TSOT23-6 FC package
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V

3. Applications

- USB PD/QC chargers
- AC/DC adapters for portable devices
- Flyback SMPS with high-efficiency requirements



aaa-043990

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX81811DA	-40 °C to +125 °C	TSOT23-6	Plastic, surface-mounted package; 6 leads	SOT8061-1
NEX81812DA	-40 °C to +125 °C	TSOT23-6	Plastic, surface-mounted package; 6 leads	SOT8061-1

5. Marking

Table 2. Marking code

Type number	Marking code
NEX81811DA	ND5
NEX81812DA	ND6

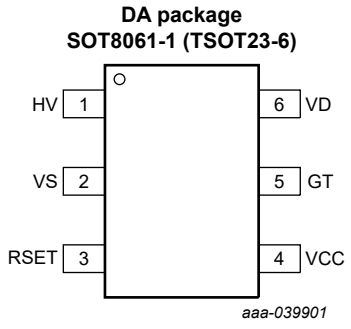
6. Device comparison

Table 3. Device comparison

Type number	Turn on blanking time (C_{SET} not installed)
NEX81811DA	1.0 µs
NEX81812DA	0.5 µs

7. Pinning information

7.1. Pinning



7.2. Pin description

Pin		I/O	Description
Name	Number		
HV	1	I	HV linear regulator input
VS	2	-	Ground reference
RSET	3	-	Configuration pin for turn-on detection and t_{on} min setting
VCC	4	-	Internal power supply
GT	5	O	Output to drive MOSFET
VD	6	O	MOSFET drain voltage sense

8. Product specifications

8.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VS (ground = 0 V).
[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	+14.0	V
GT	gate driver output		-0.3	+14.0	V
V_D	MOSFET drain voltage sense		-1.0	120	V
HV	HV linear regulator input		-1.0	120	V
RSET	turn-on detection		-0.3	6.5	V
T_{stg}	storage temperature		-55	150	°C
ESD					
V_{ESD}	ESD voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	+2000	V
		CDM: ANSI/ESDA/JEDEC JS-001 class C2a	-500	+500	V

[1] Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Section 8.3. Exposure to these limiting values for extended periods may affect device reliability.

8.2. Thermal characteristics

Table 5. Thermal characteristics

For more information about thermal metrics consult application note.

Symbol	Parameter	package 1	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	112	K/W
$R_{\Theta JC(BOT)}$	junction-to-case (bottle) thermal resistance	78	K/W

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to VS (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	13.0	V
GT	gate driver output		-0.3	10.0	V
V_D	MOSFET drain voltage sense		-1.0	100	V
HV	HV linear regulator input		-1.0	100	V
RSET	turn-on detection		-0.3	5.0	V
T_J	operation junction temperature		-40	125	°C

8.4. Recommended components

Table 7. Recommended components

Nominal component values, not including derating factors.

Symbol	Parameter		Min	Typical	Max	Unit
C_{VCC}	capacitance on VCC		0.047	0.1	2.2	µF
C_{SET}	capacitance on RSET		-	NC	-	nF
R_{SET}	resistance on RSET		0	36	200	kΩ

8.5. Electrical characteristics

Table 8. Static characteristics

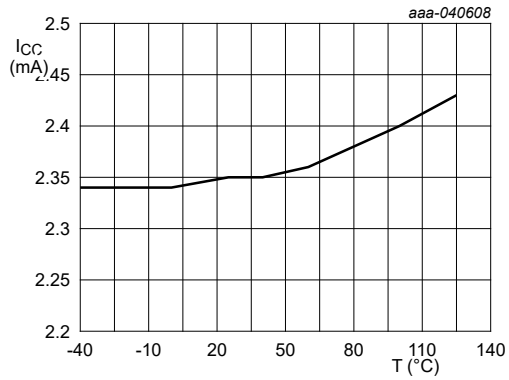
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply management section						
V_{CC_ON}	V_{CC} supply voltage	VCC supply voltage (turn-on)	4.0	4.5	5.0	V
V_{CC_OFF}		VCC supply voltage (turn-off)	3.5	4.0	4.5	V
V_{CC_HYS}	V_{CC_UVLO} hysteresis		-	0.5	-	V
I_{VCC_CHG}	VCC maximum charging current	V_{CC} = 7 V; HV = 20 V	-	70	-	mA
		V_{CC} = 4 V; V_D = 30 V; HV = 0 V	-	40	-	mA
VCC_REG	VCC regulation voltage	V_D = 12 V; HV = 12 V	8	9	10	V
		V_D = 12 V; HV = 3 V	5.5	6	6.5	V
I_{CC}	current consumption	V_{CC} = 9 V; C_{LOAD} = 2.2 nF; F_{sw} = 100 kHz	-	2.3	3	mA
		V_{CC} = 6 V; C_{LOAD} = 2.2 nF; F_{sw} = 100 kHz	-	1.4	1.8	mA
I_{CC_UVLO}	current consumption under UVLO	V_{CC} = UVLO - 0.1 V	-	40	60	µA
Control circuitry section						
V_{REG1}	1st step regulation voltage (V_{DS})		-50	-35	-20	mV
V_{REG2}	2nd step regulation voltage (V_{DS})		-200	-150	-100	mV
V_{th_ON}	turn-on threshold (V_{DS})	V_D falling	-200	-150	-80	mV
V_{th_OFF}	turn-off threshold (V_{DS})	V_D rising	-12	-3	6	mV
t_{d_ON}	turn-on delay	C_{LOAD} = 2.2 nF	-	35	-	ns
t_{d_OFF}	turn-off delay	C_{LOAD} = 2.2 nF	-	20	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d\_OFF(prop)}$	turn-off propagation delay		[1]	-	10	-	ns
t_{b_on}	turn-on blanking time	C_{SET} is not installed	NEX81811DA	-	1.0	-	µs
			NEX81812DA	-	0.5	-	µs
		C_{SET}= 1 nF	NEX81811DA	-	1.5	-	µs
			NEX81812DA	-	1.0	-	µs
		C_{SET}= 22 nF	NEX81811DA	-	2.0	-	µs
			NEX81812DA	-	1.5	-	µs
Gate driver							
V_{GT_L}	V_{GT} (low)	I_{LOAD} = 10 mA		-	0.01	0.02	V
V_{GT_H}	V_{GT} (high)	I_{LOAD} = 0 mA		-	V_{CC}	-	V
I_{GT_PU}	gate driver maximum source current			-	1	-	A
I_{GT_PD}	gate driver maximum sink current			-	4	-	A
R_{PU}	pull-up impedance			-	2.8	4.2	Ω
R_{PD}	pull-down impedance			-	0.4	0.9	Ω

[1] Guaranteed by characterization and design.

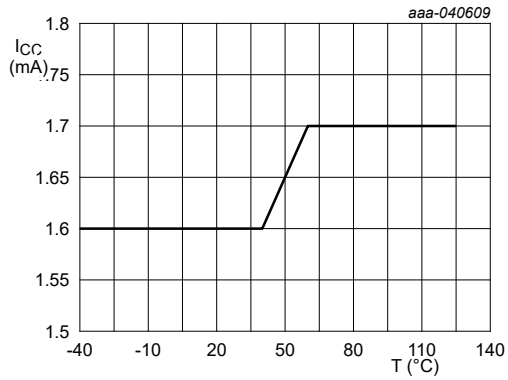
8.6. Typical characteristics

Table 9. Typical characteristics



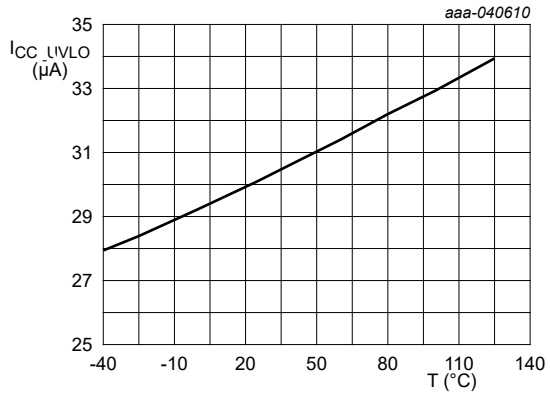
V_{CC} = 9 V, C_{LOAD} = 2.2 nF, F_{SW} = 100 kHz

Fig. 1. Operating current vs. temperature



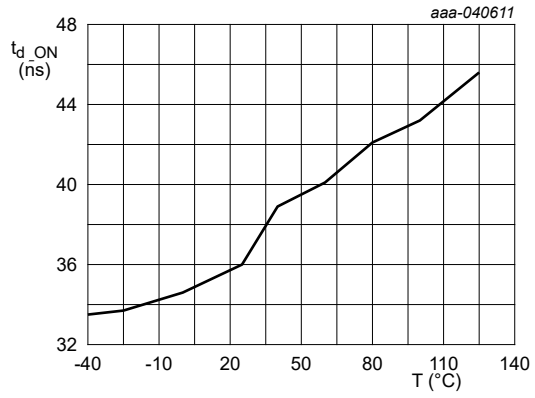
V_{CC} = 6 V, C_{LOAD} = 2.2 nF, F_{SW} = 100 kHz

Fig. 2. Operating current vs. temperature



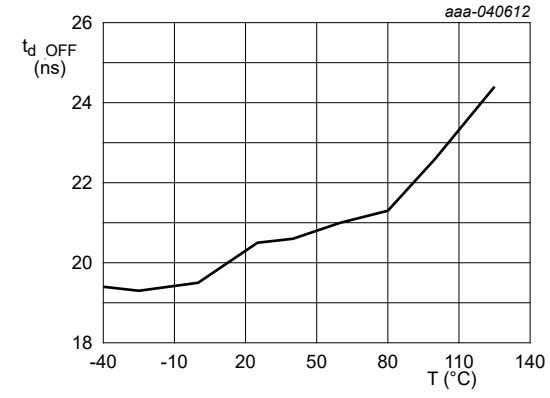
V_{CC} = 4 V

Fig. 3. V_{CC} shutdown current vs. temperature



V_{CC} = 9 V, C_{LOAD} = 2.2 nF

Fig. 4. Turn-on delay vs. temperature



V_{CC} = 9 V, C_{LOAD} = 2.2 nF

Fig. 5. Turn-off delay vs. temperature

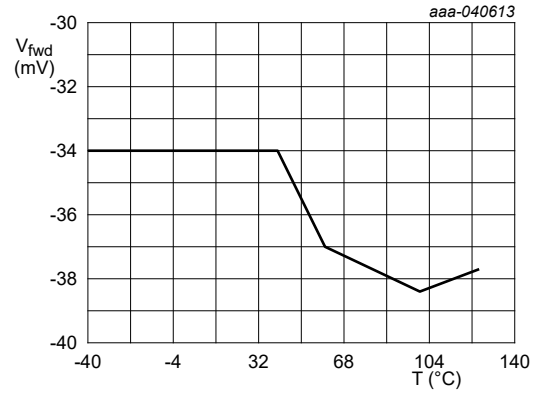


Fig. 6. First step regulation voltage vs. temperature

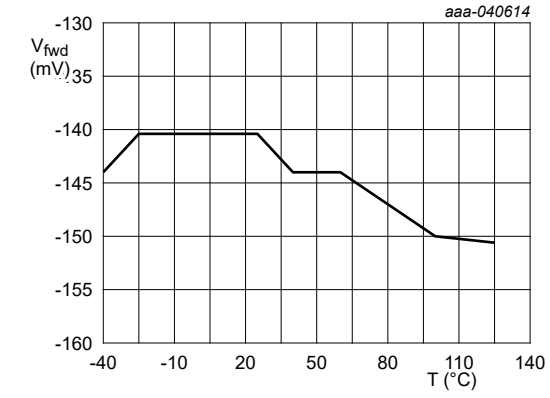
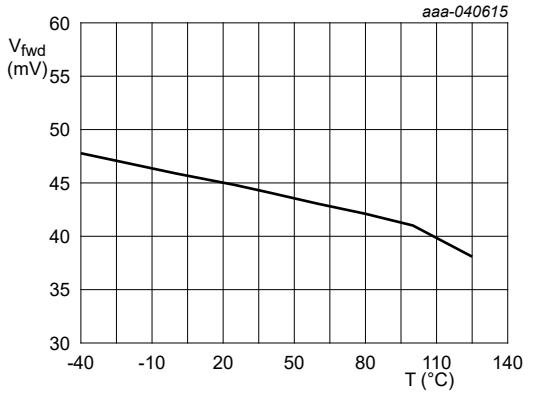
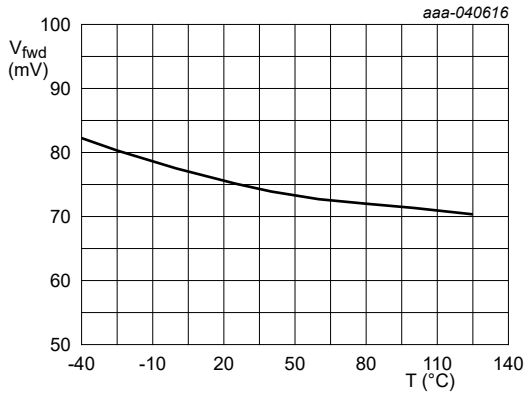


Fig. 7. Second step regulation voltage vs. temperature



V_{CC} = 4 V, V_D = 30 V

Fig. 8. V_D maximum charging current vs. temperature

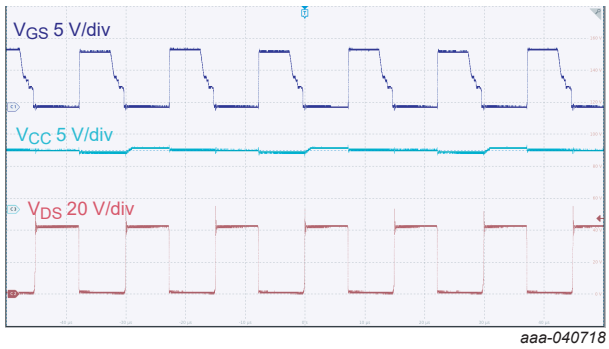


V_{CC} = 7 V, HV = 20 V

Fig. 9. HV maximum charging current vs. temperature

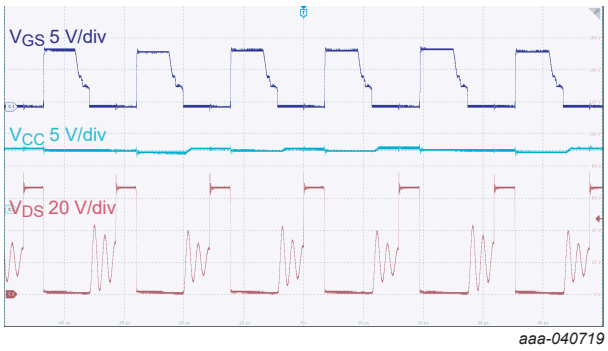
8.7. Typical waveforms

Table 10. Typical waveforms



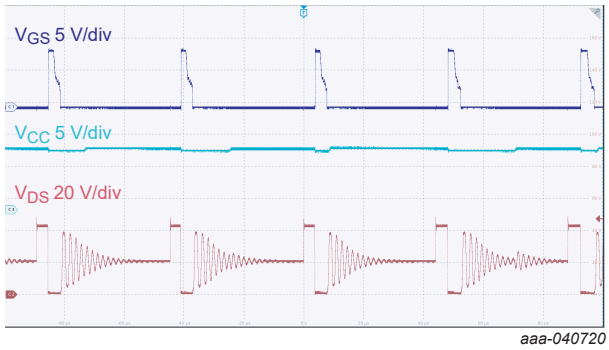
V_{IN} = 110V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
High-side, HV connected to VD

Fig. 10. Operation in 65 W flyback application



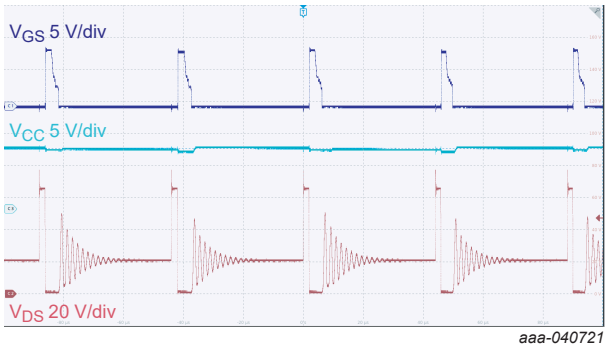
V_{IN} = 230V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
High-side, HV connected to VD

Fig. 11. Operation in 65 W flyback application



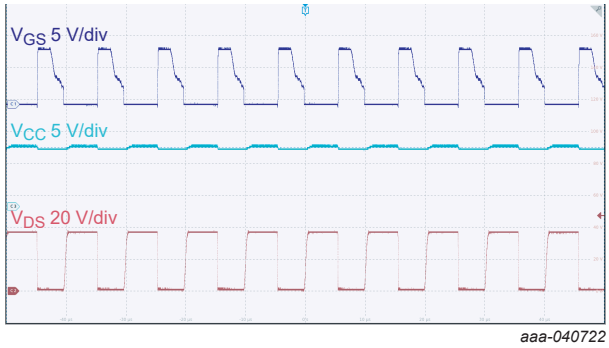
V_{IN} = 110V_{AC}, V_{OUT} = 20 V, I_{OUT} = 0.325 A
High-side, HV connected to VD

Fig. 12. Operation in 65 W flyback application



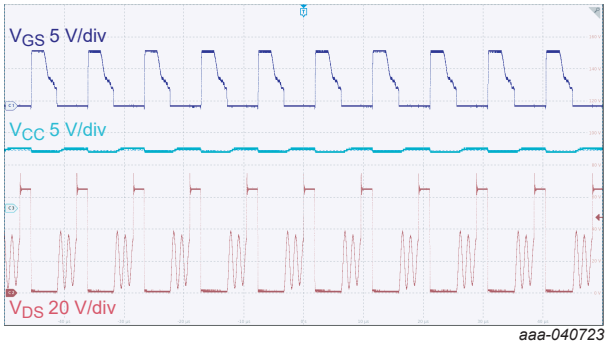
V_{IN} = 230V_{AC}, V_{OUT} = 20 V, I_{OUT} = 0.325 A
High-side, HV connected to VD

Fig. 13. Operation in 65 W flyback application



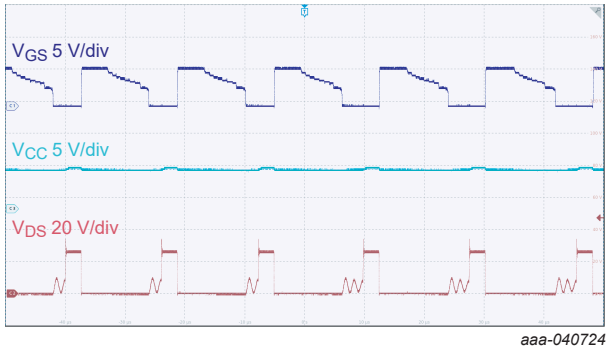
V_{IN} = 110V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
Low-side, HV connected to V+

Fig. 14. Operation in 65 W flyback application



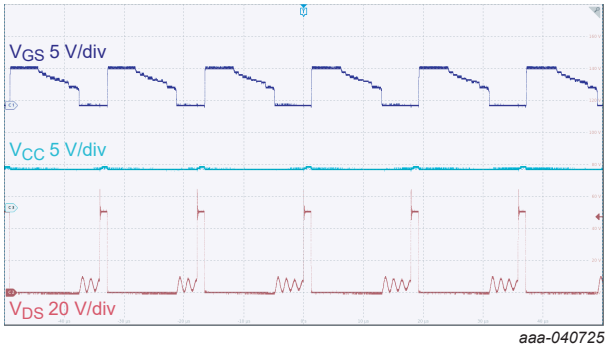
V_{IN} = 230V_{AC}, V_{OUT} = 20 V, I_{OUT} = 3.25 A
Low-side, HV connected to V+

Fig. 15. Operation in 65 W flyback application



V_{IN} = 110V_{AC}, V_{OUT} = 5 V, I_{OUT} = 3.25 A
Low-side, HV connected to V+

Fig. 16. Operation in 65 W flyback application



V_{IN} = 230V_{AC}, V_{OUT} = 5 V, I_{OUT} = 3.25 A
Low-side, HV connected to V+

Fig. 17. Operation in 65 W flyback application

9. Detailed Description

9.1. Overview

The NEX81811/2DA is designed to operate with CCM, critical conduction mode (CrM), and DCM flyback converters. The control circuitry turns on the MOSFET when the voltage on V_{DS} drops below the turn-on threshold V_{th_ON}, and turns off the MOSFET when the V_{DS} rises above the turn-off threshold V_{th_OFF}, which is typically 0 V. The IC supports both high-side and low-side SR applications.

9.2. Functional block diagram

The NEX81811/2DA functional block diagram is shown in Fig. 18:

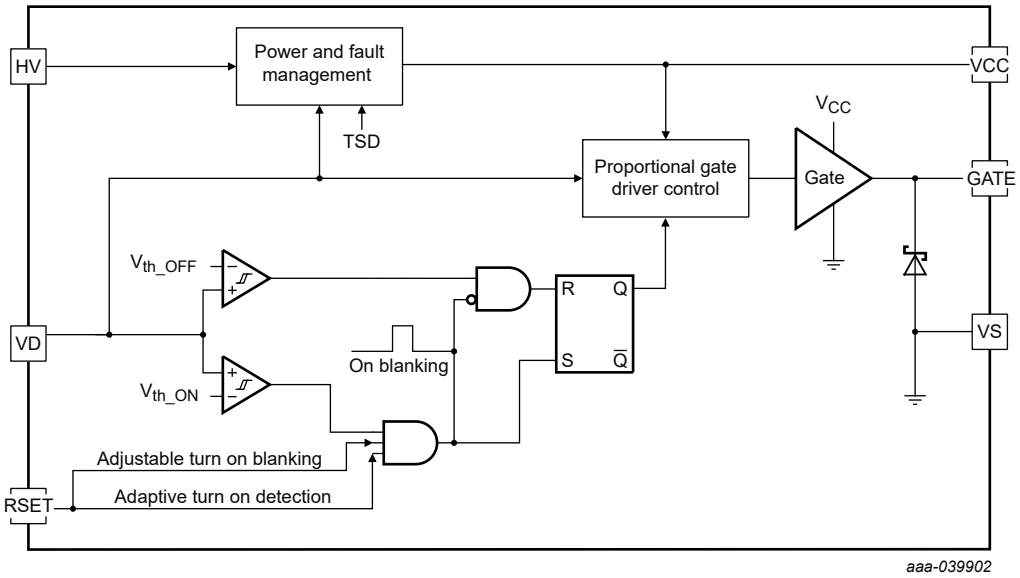


Fig. 18. Functional block diagram

9.3. Feature description

9.3.1. Supply section

When V_{CC} rises above 4.5 V, the NEX81811/2DA is enabled and exits under-voltage lockout (UVLO). When V_{CC} drops below 4.0 V, the IC enters UVLO and stops working. The UVLO hysteresis is 500 mV. A capacitor (typically 100 nF) on VCC can be used to set the startup time.

The capacitor at VCC supplies power for the IC and can be charged by both HV and VD.

If V_{HV} is less than 6.7 V, V_{CC} is regulated to 6 V.

If V_{HV} is between 6.7 V and 9.7 V, V_{CC} is regulated to VHV - 0.7 V.

If V_{HV} is higher than 9.7 V, V_{CC} is regulated to 9 V.

9.3.2. Turn-on section

An adaptive turn-on detection circuit monitors the SR MOSFET V_{DS} waveform. Once the waveform meets the turn-on criteria, the SR MOSFET will be turned on after a turn-on delay time. In DCM operation, when the magnetizing inductor current drops to zero, an oscillation waveform can be observed at V_{DS} of SR MOSFET. Sometimes the oscillation may ring below 0 V and cause the SR MOSFET to be turned on by mistake. To prevent this, NEX81811/2DA uses a circuit with an adaptive turn-on mechanism. The shorter the SR turn-off time is, the stricter the requirement is used to turn on SR MOSFET. This prevents the MOSFET from conducting during DCM ringing.

When the circuit operates under light load conditions, the SR will turn off for a longer time, which relaxes the requirements for the SR to be turned on. By this means, the SR MOSFET can be turned on normally and the light load efficiency is improved.

9.3.3. Adjustable turn-on blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on-state lasts for a predetermined length of time. The default turn-on blanking time of NEX81811DA is 1.0 µs, which is suitable for low-frequency applications. The default turn-on blanking time of NEX81812DA is 0.5 µs, which is suitable for high-frequency

applications. The turn-on blanking time can be adjusted by adding MLCC (C_{SET}) in parallel with RSET to prevent accidental shutdown in case of excessive inductance on the lead wires of the SR MOSFET and the printed circuit board (PCB), or excessive oscillation between parasitic capacitances and transformer leakage inductance. The relationship between blanking time and C_{SET} is shown in Table 11.

Table 11. NEX81811 t-blanking setting

	C_{SET}	R_{SET} (Ω)	Turn-on blanking time (µs)
NEX81811	not installed	0 Ω to 200 kΩ; 0 Ω recommended	1.0
	1.0 nF-3.3 nF	0 Ω to 200 kΩ; 36 kΩ recommended	1.5
	10 nF-27 nF		2.0

Table 12. NEX81812 t-blanking setting

	C_{SET}	R_{SET} (Ω)	Turn-on blanking time (µs)
NEX81812	not installed	0 Ω to 200 kΩ; 0 Ω recommended	0.5
	1.0 nF-3.3 nF	0 Ω to 200 kΩ; 36 kΩ recommended	1.0
	10 nF-27 nF		1.5

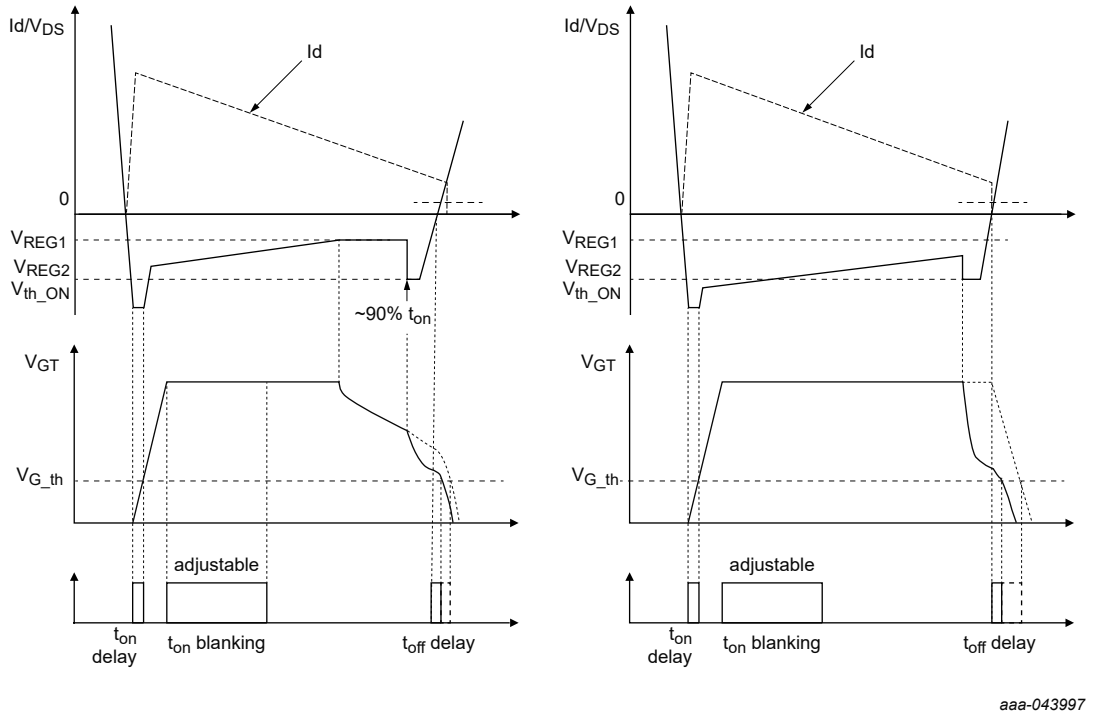


Fig. 19. Turn on/off timing

9.3.4. Conduction section

When V_{DS} rises above the first regulation step (-35mV), the gate voltage of the SR MOSFET will decrease to regulate V_{DS} to this threshold. At 90% t_{on}, NEX81811/2DA further reduces the gate voltage level to adjust V_{DS} to the second adjustment threshold (-150mV). When the V_{DS} turn off threshold is triggered, the SR MOSFET will turn off very quickly because the gate voltage is very close to the gate turn off threshold.

When the circuit operates under deep CCM conditions, or when a high RDS_{ON} MOSFET is selected, the first regulation threshold may not be triggered, but the circuit still has a chance to trigger to the second regulation threshold, thus still achieving fast turn off speed.

9.3.5. Turn-off section

The turn-off threshold is triggered when V_{DS} rises to 0 mV. Adaptive regulation control pulls the gate driver voltage (V_{GS}) to 0 mV after a very short 10 ns turn-off delay. When V_{GS} is pulled to 0 mV, a turn-off blanking time is applied, during which the gate driver signal is latched off.

10. Application Information

10.1. Application information

The following section discusses the external components required to complete the power supply design for several input and output voltage options, using the typical applications as a reference.

10.2. Typical system implementation

The NEX81811/2DA can support both high-side and low-side applications.

Fig. 20 shows the typical low-side implementation with standard level MOSFET. In this situation, V_{CC} is regulated to V_{HV} - 0.7 V. The maximum value of V_{CC} is 9 V.

Fig. 21 shows the typical low-side implementation with logic level MOSFET; V_{CC} is regulated to 6 V.

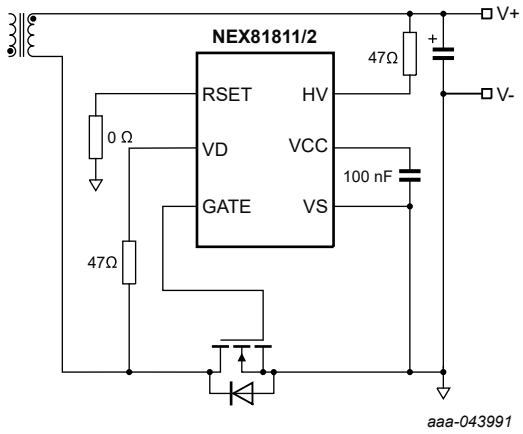


Fig. 20. Low-side with standard level MOSFET

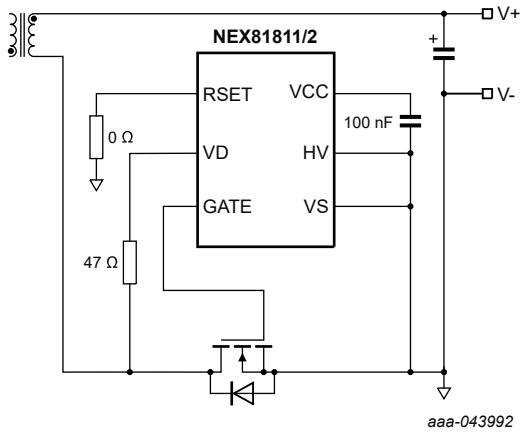


Fig. 21. Low-side with logic level MOSFET

Fig. 22 shows the typical high-side implementation with standard level MOSFET; V_{CC} is regulated to 9 V.

Fig. 23 shows the typical high-side implementation with standard level MOSFET, high voltage output; V_{CC} is regulated to 9 V (suitable for high voltage output applications).

Fig. 24 shows the typical high-side implementation with logic level MOSFET; V_{CC} is regulated to 6 V.

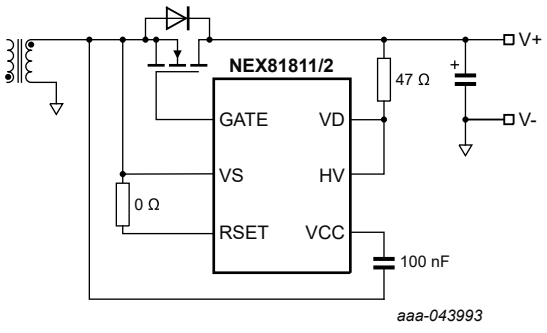


Fig. 22. High-side with standard level MOSFET

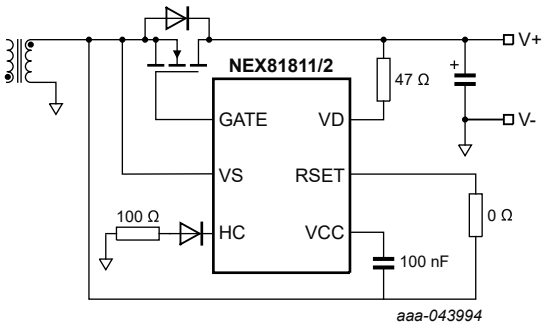


Fig. 23. High-side with standard level MOSFET

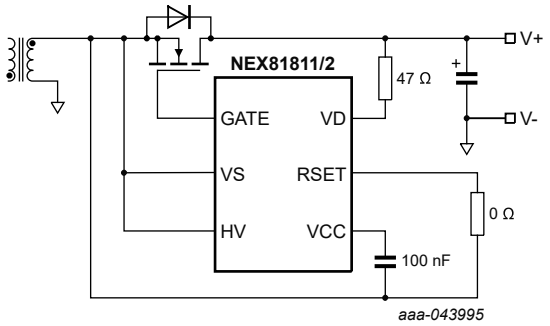


Fig. 24. High-side with logic level MOSFET

10.3. External resistor selection

To prevent high negative voltage on the VD and HV pins from damaging the device, an external resistor needs to be in series to VD and HV. The resistor can also protect the IC from ESD damage. Generally, a resistance between 10-100 Ω is recommended.

The adaptive turn-on mechanism means that RSET can directly short to GND, to better prevent the circuit from misconducting by DCM ringing. The resistance is recommended to be less than 200 kΩ.

10.4. External capacitor selection

Normally, a capacitor with a range of 100 nF to 1 uF is needed to connect between VCC and GND. Larger VCC capacitance leads to longer start up time and larger V_{DS} spike; 100 nF or 220 nF is recommended as the VCC UVLO hysteresis 500 mV is big enough to cover the larger ripple on V_{CC}.

R_{SET} is recommended to be higher than 30 kΩ if C_{SET} is placed. For C_{SET} values, see Table 11.

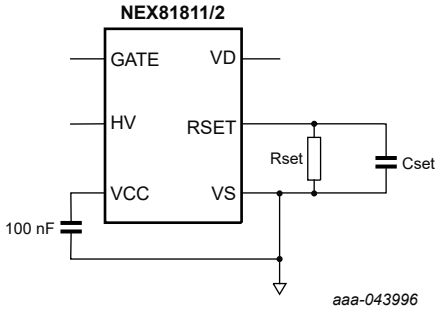


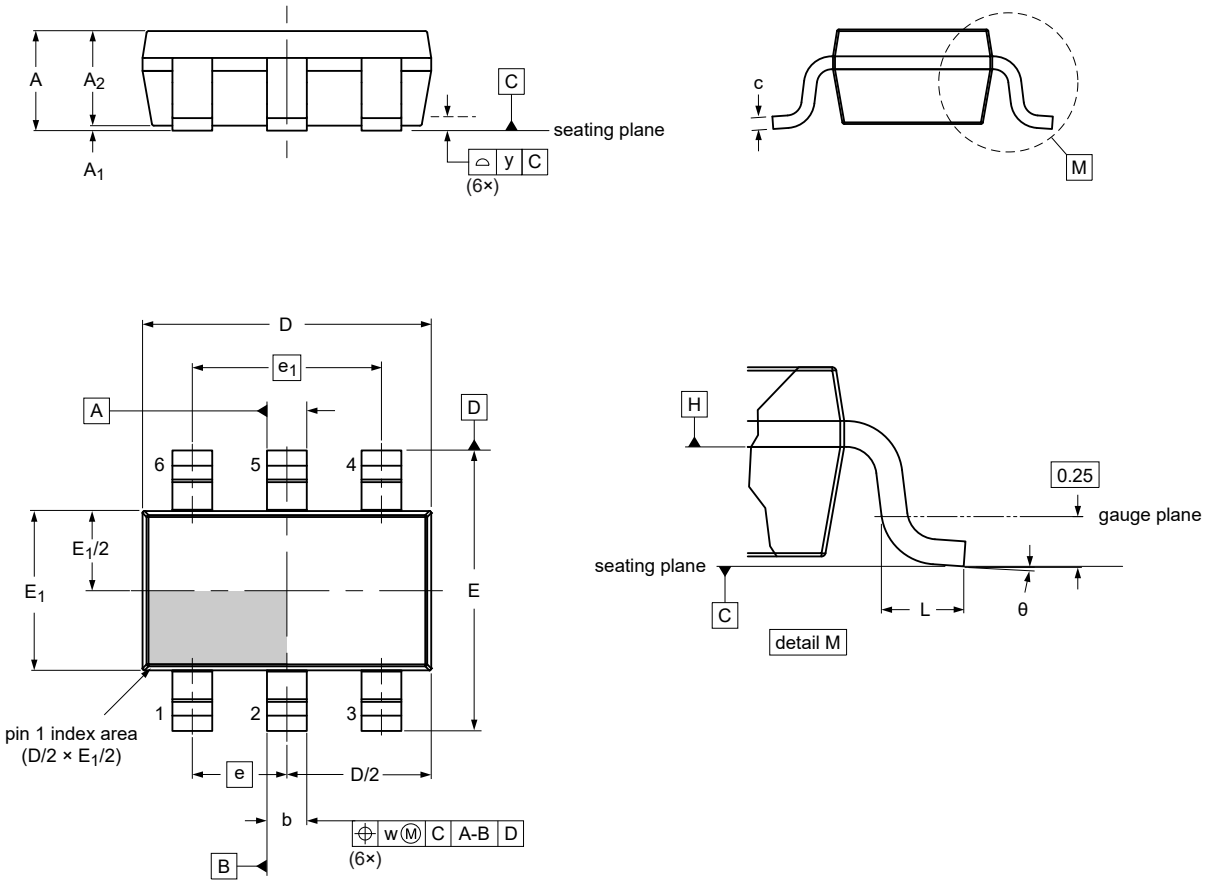
Fig. 25. C_{VCC} and C_{SET}

11. Layout

1. Make the sensing connection (VD/VS) as close as possible to the MOSFET (drain/source).
2. Make the sensing loop as small as possible. Keep the IC out of the power loop to avoid interference between the sensing loop and the power loop.
3. Place a decoupling ceramic capacitor from VCC to GND close to the IC for adequate filtering.
4. Make the gate driver loop as small as possible to minimize the parasitic inductance.
5. Keep the driver signal far away from the VD sensing trace on the layout.

12. Package outline

Plastic, surface-mounted package (TSOT23-6); 6 leads **SOT8061-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	e_1	L	y	w	θ
mm	max	1.10	0.10	1.00	0.50	0.20	3.05	3.00	1.75	0.95 BSC	1.90 BSC	0.60	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min		0.00	0.70	0.30	0.08	2.75	2.60	1.45			0.30			0°

Note
Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per end.
Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0. 25 mm per side.
D and E_1 dimensions are determined at datum H.

sot8061-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8061-1		MO-193				~~24-09-04~~ 24-09-16

Fig. 26. Package outline SOT8061-1 (TSOT23-6)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CCM	Continuous Conduction Mode
CDM	Charged Device Model
CrM	Critical conduction Mode
DCM	Discontinuous Conduction Mode
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FC	Flip Chip
HBM	Human Body Model
HV	High Voltage
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PD	USB Power Delivery
QC	Qualcomm Quick Charge
QR	Quasi-resonant
SMPS	Switched-Mode Power Supply
SR	Synchronous Rectification
USB	Universal Serial Bus
UVLO	Under-Voltage LockOut

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX81811_2DA v.1.1	20251222	Product data sheet	-	-
Modifications	• Drawing corrected in Section 3.			
NEX81811_2DA v.1	20251219	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 22 December 2025