NEX1324X-Q100

24-channel automotive linear LED driver

Rev. 1.2 — 23 October 2025 Product data sheet

1. General description

NEX1324X-Q100 is an AEC-Q100 Grade 1 qualified 24-channel, 40 V high-side LED driver with up to 100 mA output current per channel, PWM and analog dimming support, and MTP for configurable depending on application requirements in automotive lighting systems.

NEX1324X-Q100 supports 8-bit output current with high accuracy from channel to channel and device to device. Channels can be used in parallel to support higher current output than 100 mA. The low dropout of the device helps mitigate the heat generation of the device itself. The device integrates UART over CAN as the digital interface to enable long distance off-board communication, which is a typical scenario for automotive exterior lighting where different lamp functions are typically located in different PCBs. NEX1324X-Q100 also supports LED open-circuit, short to ground, and single-LED short-circuit diagnostics. Additionally, a configurable watchdog automatically sets the part into Fail-Safe state when the CAN bus connection is lost.

NEX1324X-Q100 can operate at a junction temperature ranging from -40 °C to 150 °C in a thermally enhanced 38-pin HTSSOP38 package.

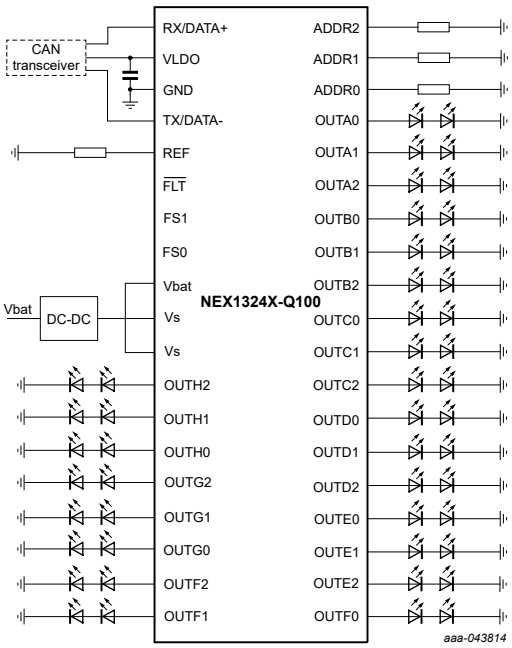

Fig. 1. Typical application

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to 125 °C
- Function safety capable
  - Provide documents to support function safety design
- 24-channel precision high-side current output:
  - V_{Vbat}: 4.5 V to 36 V; V_{Vs}: 3.8 V to 20 V
  - Up to 100 mA channel current per channel
  - 2-bit global, 6-bit independent current setting
  - Current accuracy within ±5 % from 5 mA to 100 mA
  - Low voltage drops: 600 mV at 100 mA
  - 12-bit independent PWM dimming
  - Programmable PWM frequency: 200 Hz to 23.4 kHz
  - Linear and exponential dimming method
- Integrated CAN compatible interface:
  - Data rate up to 2 Mbit/s
  - Supports UART data format
  - Supports 27 slave addresses set by resistors
- Diagnostics and protections:
  - Programmable Fail-Safe state
  - LED open-circuit detection
  - LED short-circuit detection
  - Single-LED short-circuit diagnostic
  - Programmable low-supply detection
  - Open-drain $\overline{FLT}$ pin for fault indication
  - Communication Watchdog
  - 8-bit ADC for pin voltage measurement
  - Overtemperature protection
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2b exceeds 750 V

3. Applications

- Automotive exterior rear lights
- Automotive exterior headlights

4. Ordering information

Table 1. Ordering information

Type number	Temperature range	Name	Description	Version
NEX13240PE-Q100	T_{amb} = -40 °C to 125 °C	HTSSOP38	plastic, thermal enhanced thin shrink small outline package; 38 leads; 0.5 mm pitch; 9.7 mm x 4.4 mm x 1.2 mm body	SOT8106-1
NEX13241PE-Q100				

5. Marking

Table 2. Marking

Type number	Marking code
NEX13240PE-Q100	N13240
NEX13241PE-Q100	N13241

6. Device comparison

Table 3. Device Comparison

Type number	Key features
NEX13240PE-Q100	24-channel + UART + FS capable
NEX13241PE-Q100	24-channel + CAN + FS capable
NEX13160PE-Q100	16-channel + UART + FS capable
NEX13161PE-Q100	16-channel + CAN + FS capable

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7. Application block diagram

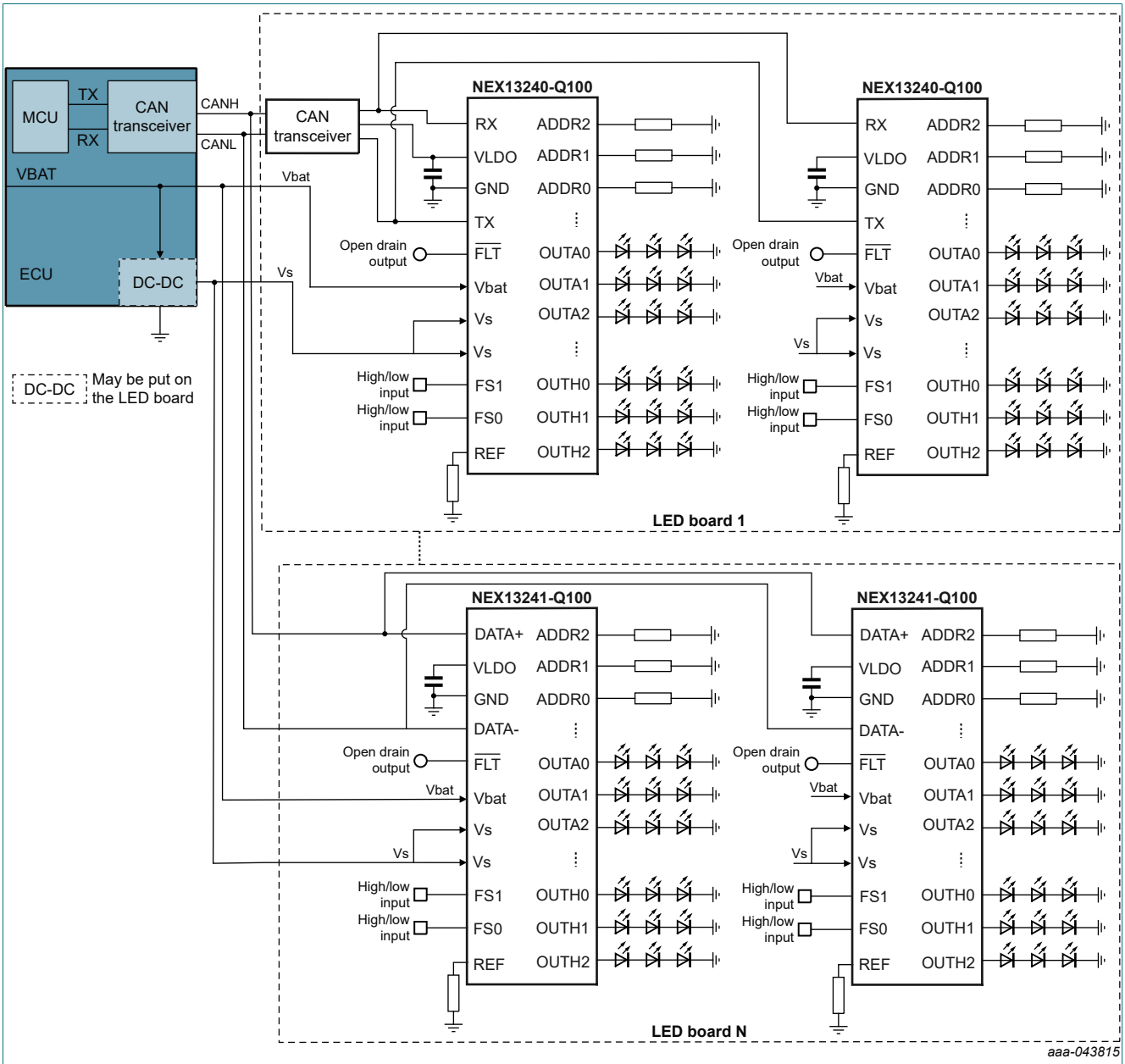

Fig. 2. Application block diagram

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8. Pinning information

8.1. Pin configuration

Table 4. Pin configuration SOT8106-1 (HTSSOP38)

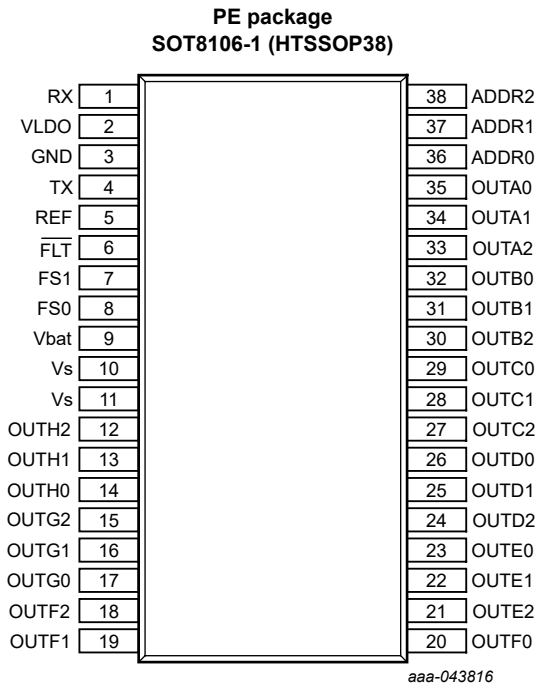

Fig. 3. NEX13240-Q100 pin configuration

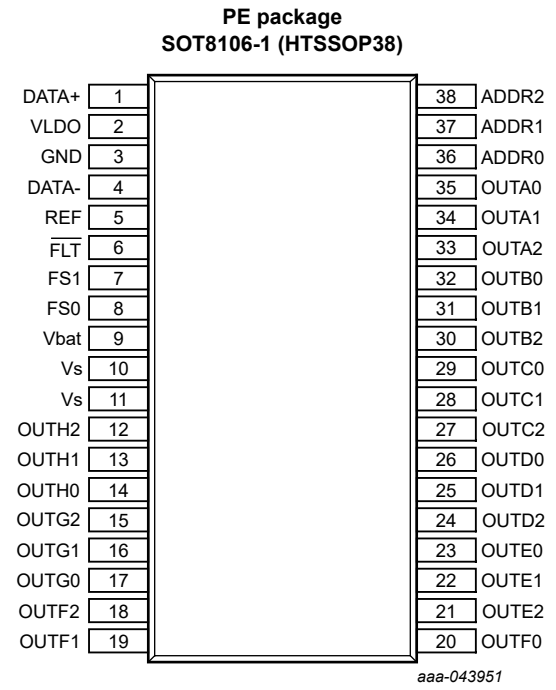

Fig. 4. NEX13241-Q100 pin configuration

8.2. Pin description

Symbol	Pin	I/O	Description
RX[1]	1	I	UART RX over CAN physical layer[1]
DATA+[2]			differential interface positive[2]
VLDO	2	Power	output of internal 5 V LDO
GND	3	GND	device ground
TX[1]	4	O	UART TX over CAN physical layer[1]
DATA-[2]			differential interface negative[2]
REF	5	I/O	device reference current setting, MTP programming chip-selection input
$\overline{FLT}$	6	I/O	open-drain error output
FS1	7	I	Fail-Safe input 1
FS0	8	I	Fail-Safe input 0
Vbat	9	Power	power supply for internal circuit
Vs	10	Power	power supply for current output channels
Vs	11	Power	power supply for current output channels
OUTH2 to OUTH0	12 to 14	O	current output channel H2 to H0
OUTG2 to OUTG0	15 to 17	O	current output channel G2 to G0
OUTF2 to OUTF0	18 to 20	O	current output channel F2 to F0

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Symbol	Pin	I/O	Description
OUTE2 to OUTE0	21 to 23	O	current output channel E2 to E0
OUTD2 to OUTD0	24 to 26	O	current output channel D2 to D0
OUTC2 to OUTC0	27 to 29	O	current output channel C2 to C0
OUTB2 to OUTB0	30 to 32	O	current output channel B2 to B0
OUTA2 to OUTA0	33 to 35	O	current output channel A2 to A0
ADDR0	36	I	device address 0
ADDR1	37	I	device address 1
ADDR2	38	I	device address 2

[1] NEX13240-Q100
[2] NEX13241-Q100

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pin Vbat	-0.3	45	V
		pin Vs	-0.3	22	V
		pins DATA+, DATA-	-0.3	20	V
		pins REF, ADDRn	-0.3	5.5	V
V_O	output voltage	pins OUTXn	-0.3	V_{Vs} + 0.3	V
		pin VLDO	-0.3	5.5	V
$V_{I/O}$	I/O voltage	pins FS0, FS1	-0.3	V_{Vbat} + 0.3	V
		pin $\overline{FLT}$	-0.3	20	V
		pins RX, TX	-0.3	5.5	V
T_j	junction temperature		-40	150	°C
T_{amb}	ambient temperature		-40	125	°C
T_{stg}	storage temperature		-65	150	°C

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10. ESD Ratings

Table 6. ESD ratings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 3B	[1][2]	-14000	-	14000	V
		HBM: ANSI/ESDA/JEDEC JS-001 class 3A	[2][3]	-4000	-	4000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2b	[4]	-750	-	750	V

[1] Pin DATA+, DATA-.
[2] HBM stress testing was performed in accordance with AEC-Q100-002.
[3] Rest pins.
[4] CDM stress testing was performed in accordance with AEC-Q100-011.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{Vbat}	input voltage	pin Vbat; device supply voltage	4.5	-	36	V
V_{Vs}	input voltage	pin Vs; power supply for output current channel	3.8	-	20	V
I_{OUTXn}	output current	pins OUTXn; channel output current	-	-	100	mA
V_{FS0}, V_{FS1}	input voltage	pin FS0, FS1; external Fail-Safe selection input	0	-	V_{Vbat}	V
V_{RX}	UART input	pin RX	0	-	5	V
V_{TX}	UART output	pin TX	0	-	5	V
V_{DATA+}	differential interface positive	pin DATA+	0	-	5	V
V_{DATA-}	differential interface negative	pin DATA-	0	-	5	V
V_{VLDO}	VLDO voltage	pin VLDO; internal 5 V VLDO output	0	-	5	V
I_{VLDO}	VLDO current	pin VLDO; current capability	0	-	80	mA
V_{ADDRn}	input voltage	pins ADDRn; device address selection	0	-	5	V
V_{REF}	pin REF	current reference setting	0	-	5	V
$V_{\overline{FLT}}$	pin $\overline{FLT}$	error feedback open-drain output	0	-	20	V
$f_{bd(UART)}$	UART baud rate		0.1	-	2	Mbps
T_{amb}	ambient temperature		-40	-	125	°C
T_j	junction temperature		-40	-	150	°C

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12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	SOT8106-1 (HTSSOP38)	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	28.6	°C/W
$R_{\Theta JC(TOP)}$	junction-to-case (top) thermal resistance	18.3	°C/W
$R_{\Theta JB}$	junction-to-board thermal resistance	11.3	°C/W
Θ_{JT}	junction-to-top char parameter	0.5	°C/W

13. Electrical characteristics

Table 9. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
Bias						
V_{Vbat}	operating input voltage range		4.5	12	40[1]	V
$I_{q(Vbat)}$	quiescent current, all-channels ON	V_{Vbat} = 12 V; R_{REF} = 8.45 kΩ; all outputs ON; REFRANGE = 11b; PWM duty = 0	-	7.5	10	mA
	quiescent current, all-channels OFF	V_{Vbat} = 12 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; all outputs OFF	-	7.5	10	mA
$I_{q(Vs)}$	quiescent current, all-channels ON	V_{Vbat} = 12 V; V_{Vs} = 12 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; PWM Duty = 0; all outputs ON	-	8.5	10	mA
	quiescent current, all-channels-off	V_{Vbat} = 12 V; V_{Vs} = 12 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; all outputs OFF	-	22	50	µA
$I_{fault(Vbat)}$	quiescent current, Fail-Safe state fault mode	V_{Vbat} = 12 V; Fail-Safe state; all outputs OFF; $\overline{FLT}$ = LOW	-	7.5	10	mA
$I_{fault(Vs)}$	quiescent current, Fail-Safe state fault mode	V_{Vbat} = 12 V; V_{Vs} = 12 V; Fail-Safe state; all outputs OFF; $\overline{FLT}$ = LOW	-	22	50	µA
$I_{LKG(Vs)}$	Vs leakage current	V_{Vs} = 20 V; V_{Vbat} = 0 V	-	-	5	µA
$V_{Vbat\_POR\_rise}$	Vbat power-on-reset rising threshold		3.95	4.2	4.48	V
$V_{Vbat\_POR\_fall}$	Vbat power-on-reset falling threshold		3.65	3.85	4.1	V
$V_{O(VLDO)}$	VLDO output voltage	V_{Vbat} > 5.6 V; I_{VLDO} = 40 mA	4.75	5	5.25	V
$I_{O(VLDO)}$	VLDO output current capability		-	-	80	mA
I_{VLDO_limit}	VLDO output current limit		110	-	-	mA
V_{LDO_drop}	LDO maximum dropout voltage	V_{Vbat} = 4.9 V; I_{VLDO} = 80 mA	-	0.55	0.9	V
		V_{Vbat} = 4.9 V; I_{VLDO} = 50 mA	-	0.35	0.6	V
$V_{VLDO\_POR\_rise}$	VLDO power-on-reset rising threshold		3	3.2	3.5	V
$V_{VLDO\_POR\_fall}$	VLDO power-on-reset falling threshold		2.75	3	3.25	V

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Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
$V_{VLDO\_OV\_rise}$	VLDO overvoltage rising threshold		5.7	6	6.5	V
$V_{VLDO\_OV\_fall}$	VLDO overvoltage falling threshold		5.5	5.75	6.2	V
C_{VLDO}	supported VLDO loading capacitance		1	-	10	µF
f_{osc}	internal oscillator frequency		-2.5%	12	2.5%	MHz
$\overline{FLT}$						
$V_{IL(FLT)}$	logic low voltage, $\overline{FLT}$		-	-	1	V
$V_{IH(FLT)}$	logic high voltage, $\overline{FLT}$		1.3	-	-	V
$I_{pd(FLT)}$	$\overline{FLT}$ pull-down current capability	$V_{\overline{FLT}}$ = 0.4 V	3	6	9	mA
$I_{LKG(FLT)}$	$\overline{FLT}$ leakage current	$V_{\overline{FLT}}$ = 5 V	-	-	1	µA
Differential data interface						
$V_{O(DOM)}$	DATA+ output voltage (dominant)	V_{Vbat} = 12 V	2.75	-	4.5	V
	DATA- output voltage (dominant)	V_{Vbat} = 12 V	0.5	-	2.25	V
$V_{O(DOM)\_diff}$	Differential output voltage (dominant)	VLDO = 5 V; DATA+ - DATA-	1.5	-	3	V
$V_{O(REC)\_diff}$	DATA+, DATA- output voltage (recessive)	VLDO = 5 V; DATA+; DATA-	2	0.5 x VLDO	3	V
	differential output voltage (recessive)	VLDO = 5 V; DATA+ - DATA-	-0.5	-	0.05	V
UART interface						
$V_{IL(RX)}$	input logic low voltage, RX		-	-	0.7	V
$V_{IH(RX)}$	input logic high voltage, RX		2	-	-	V
$V_{OL(TX)}$	low-level output voltage TX,	I_{sink} = 5 mA	0	-	0.3	V
$V_{OH(TX)}$	high-level output voltage TX,	I_{source} = 5 mA; $V_{pull\text{-}up}$ = VLDO	4.5	-	5.1	V
$I_{LKG(TX,RX)}$	TX, RX leakage current	V_{RX} = 5 V; V_{TX} = 5 V	-1	-	1	µA
ADDRn, FSn						
$V_{IL(FS)}$	input logic low voltage, FS		-	-	0.95	V
$V_{IH(FS)}$	input logic high voltage, FS		1.3	-	-	V
$R_{PD(FS)}$	internal pull-down resistance, FS	VLDO = 5 V	-	100	-	kΩ
$V_{IL(ADDRn)}$	logic low voltage ADDR2, ADDR1, ADDR0	VLDO = 5 V	-	-	0.65	V
$V_{IM(ADDRn)}$	logic middle voltage ADDR2, ADDR1, ADDR0	VLDO = 5 V	0.9	-	1.5	V
$V_{IH(ADDRn)}$	logic high voltage ADDR2, ADDR1, ADDR0	VLDO = 5 V	2	-	-	V
R_{ADDRn}	pull-up resistor		-	90	-	kΩ
ADC						
DNL	differential non-linearity		-1	-	1	LSB
INL	differential non-linearity		-2	-	2	LSB

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Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
Output drivers						
f_{PWM}	PWM dimming frequency range	PWMFREQ=0	-	0.2	-	kHz
		PWMFREQ=15	-	23.4	-	kHz
ΔI_{OUT_d2d}	device-to-device accuracy $\Delta I_{(OUT\_d2d)} = 1 - I_{avg(OUT)} / I_{nom(OUT)}$	V_{Vs} = 8 V; R_{REF} = 6.34 kΩ; REFRANGE = 11b; DC = 63; I_{OUT}= 100 mA	-5	0	5	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; DC = 63; I_{OUT} = 75 mA	-5	0	5	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 10b; DC = 63; I_{OUT} = 37.5 mA	-5	0	5	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 01b; DC = 63; I_{OUT} = 18.75 mA	-5	0	5	%
ΔI_{OUT_c2c}	channel-to-channel accuracy $\Delta I_{(OUT\_c2c)} = 1 - I_{(OUTn)} / I_{avg(OUT)}$	V_{Vs} = 8 V; R_{REF} = 6.34 kΩ; REFRANGE = 11b; DC = 63; I_{OUT} = 100 mA	-4	0	4	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; DC = 63; I_{OUT} = 75 mA	-4	0	4	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 10b; DC = 63; I_{OUT} = 37.5 mA	-4	0	4	%
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 01b; DC = 63; I_{OUT} = 18.75 mA	-5	0	5	%
V_{OUT_drop}	output dropout voltage	V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; DC = 38; I_{OUT} = 45 mA	-	350	550	mV
		V_{Vs} = 8 V; R_{REF} = 8.45 kΩ; REFRANGE = 11b; DC = 63; I_{OUT} = 75 mA	-	450	700	mV
		V_{Vs} = 8 V; R_{REF} = 6.34 kΩ; REFRANGE = 11b; DC = 63; I_{OUT} = 100 mA	-	600	850	mV
R_{REF}			5	-	50	kΩ
C_{REF}			0	-	4.7	nF
V_{REF}			-	1.235	-	V
K_{REF_11}		REFRANGE = 11b	-	512	-	-
K_{REF_10}		REFRANGE = 10b	-	256	-	-
K_{REF_01}		REFRANGE = 01b	-	128	-	-
K_{REF_00}		REFRANGE = 00b	-	64	-	-
$I_{REF\_OPEN\_th}$			-	10	-	µA
$V_{REF\_SHORT\_th}$			-	0.6	-	V
Diagnostics						
$V_{Vs\_UV\_th}$	Vs undervoltage threshold		2.45	2.85	3	V
$V_{Vs\_LOW\_th}$	Vs low threshold, LOWVSTH=0		3.8	4	4.4	V

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Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
$V_{OPEN\_th\_rise}$	LED open rising threshold, OPENTH=0, AUTOSS=0	V_{Vs} - V_{OUTn}	100	200	300	mV
	LED open rising threshold, OPENTH=1, AUTOSS=0	V_{Vs} - V_{OUTn}	200	300	400	mV
$V_{OPEN\_th\_fall}$	LED open falling threshold, OPENTH=0, AUTOSS=0	V_{Vs} - V_{OUTn}	200	300	400	mV
	LED open falling threshold, OPENTH=1, AUTOSS=0	V_{Vs} - V_{OUTn}	300	400	550	mV
$V_{OPEN\_th\_hyst}$	LED open hysteresis		-	100	-	mV
$V_{SG\_th\_rise}$	short to GND rising threshold		0.8	0.9	1	V
$V_{SG\_th\_fall}$	short to GND falling threshold		1.1	1.2	1.3	V
$V_{SG\_th\_hyst}$	short to GND hysteresis		-	0.3	-	V
$V_{SLS\_th\_rising}$	single-LED short rising threshold, SLSTHx = 0		2.3	2.5	2.75	V
$V_{SLS\_th\_falling}$	single-LED short falling threshold, SLSTHx = 0		2.5	2.8	2.95	V
$V_{SLS\_th\_hyst}$	single-LED short hysteresis, SLSTHx = 0		-	300	-	mV
MTP						
N_{MTP}	number of programming cycles		1000	-	-	-
Temperature						
T_{PRETSD}	pre-thermal warning threshold		-	135	-	°C
T_{PRETSD_HYS}	pre-thermal warning hysteresis		-	5	-	°C
T_{TSD1}	over-temperature protection threshold		-	175	-	°C
T_{TSD2}	over-temperature shutdown threshold		-	185	-	°C
T_{TSD1_HYS}	over-temperature protection hysteresis		-	15	-	°C
T_{TSD2_HYS}	over-temperature shutdown hysteresis		-	15	-	°C

[1] 40 V is only for short-time operating; long-term operating voltage should be lower than 36 V.

Table 10. Timing requirement

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
t_{BLANK}	diagnostics pulse-width, BLANK = 0h		-	100	-	µs
t_{CONV}	time needed to complete one AD conversion		-	55	-	µs
t_{retry}	fault retry timer		-	10	-	ms

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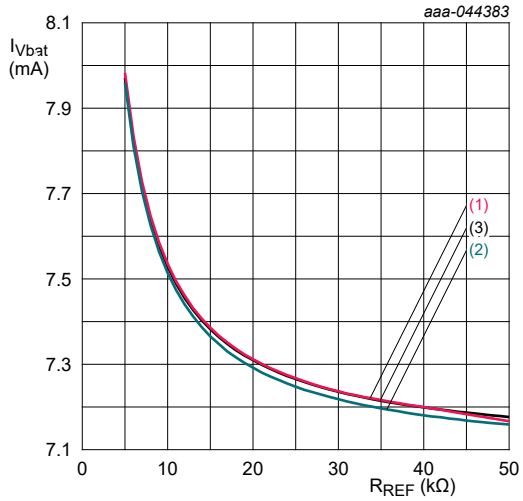
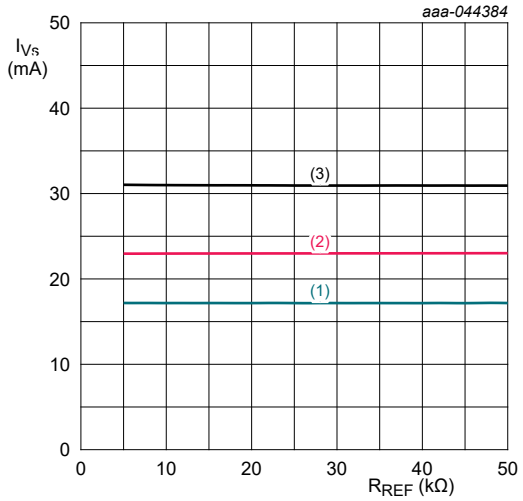
14. Typical characteristics



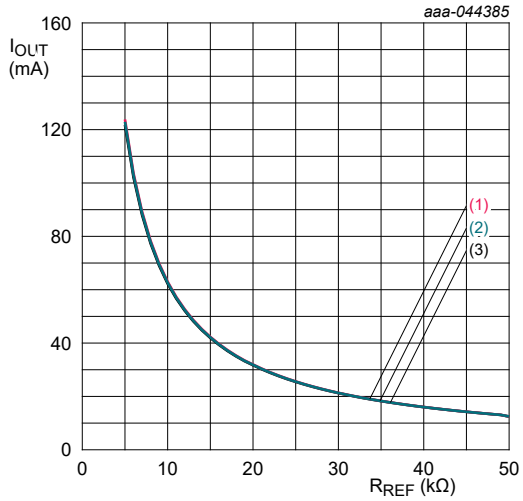
REFRANGE[1:0] = 3h
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 5. Vbat standby current versus R_{REF} resistor



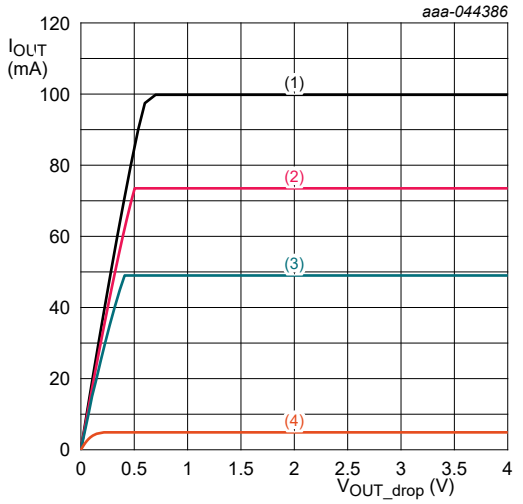
REFRANGE[1:0] = 3h
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 6. Vs standby current versus R_{REF} resistor



IOUTx[5:0] = 3Fh
REFRANGE[1:0] = 3h
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 7. Output full-range current versus R_{REF} Resistor



REFRANGE[1:0] = 3h
(1) I_{OUT} = 100 mA
(2) I_{OUT} = 75 mA
(3) I_{OUT} = 50 mA
(4) I_{OUT} = 5 mA

Fig. 8. Output current versus dropout voltage

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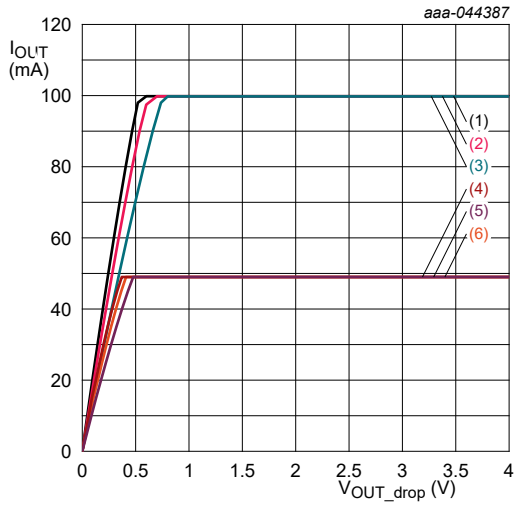
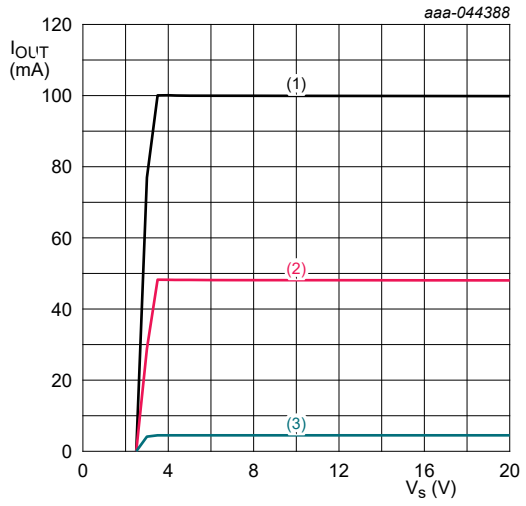


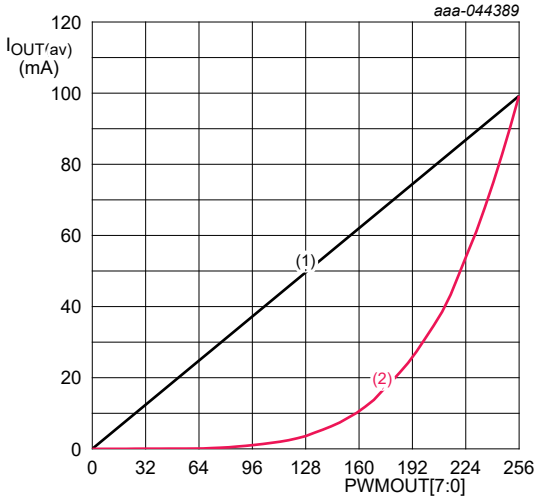
R_{REF} = 6.34 kΩ & 12.6 kΩ
REFRANGE[1:0] = 3h
(1) I_{OUT} = 100 mA; T_{amb} = -40 °C
(2) I_{OUT} = 100 mA; T_{amb} = 25 °C
(3 I_{OUT} = 100 mA; T_{amb} = 125 °C
(4) I_{OUT} = 50 mA; T_{amb} = -40 °C
(5) I_{OUT} = 50 mA; T_{amb} = 25 °C
(6) I_{OUT} = 50 mA; T_{amb} = 125 °C

Fig. 9. Output current versus dropout voltage



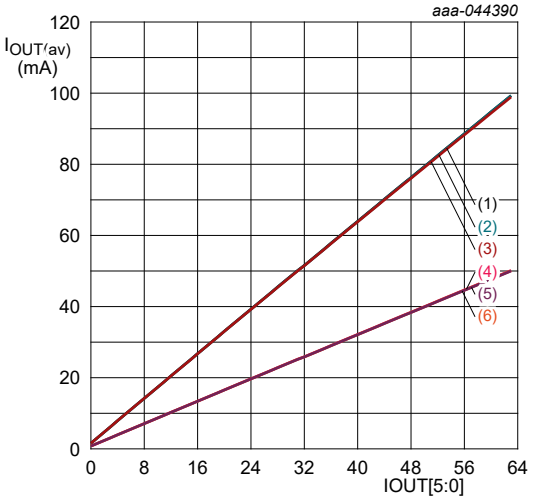
REFRANGE[1:0] = 3h
(1) I_{OUT} = 100 mA
(2) I_{OUT} = 50 mA
(3) I_{OUT} = 5 mA

Fig. 10. Output current versus Vs voltage



EXPEN = 0 & 1
IOUTx[5:0] = 3Fh
(1) CONF_EXPEN = 0
(2) CONF_EXPEN = 1

Fig. 11. Average current versus PWMOUT[7:0]



R_{REF} = 6.34 kΩ & 12.6 kΩ
REFRANGE[1:0] = 3h
(1) I_{OUT} = 100 mA; T_{amb} = -40 °C
(2) I_{OUT} = 100 mA; T_{amb} = 25 °C
(3) I_{OUT} = 100 mA; T_{amb} = 125 °C
(4) I_{OUT} = 50 mA; T_{amb} = -40 °C
(5) I_{OUT} = 50 mA; T_{amb} = 25 °C
(6) I_{OUT} = 50 mA; T_{amb} = 125 °C

Fig. 12. Output DC current versus IOUT[5:0]

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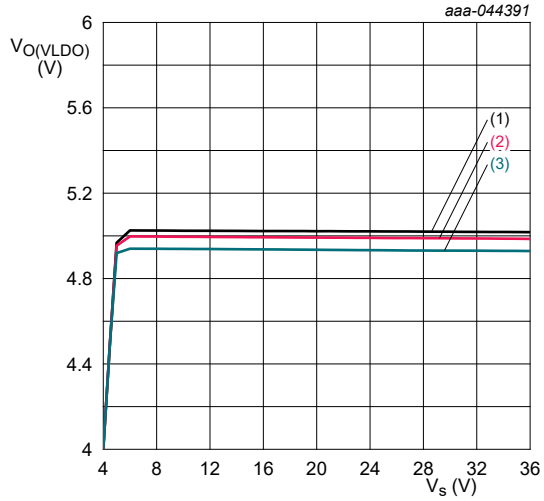

(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 13. LDO output line regulation

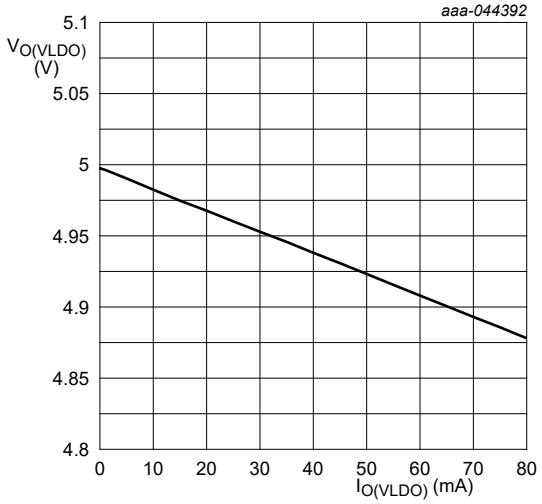

Fig. 14. LDO output load regulation

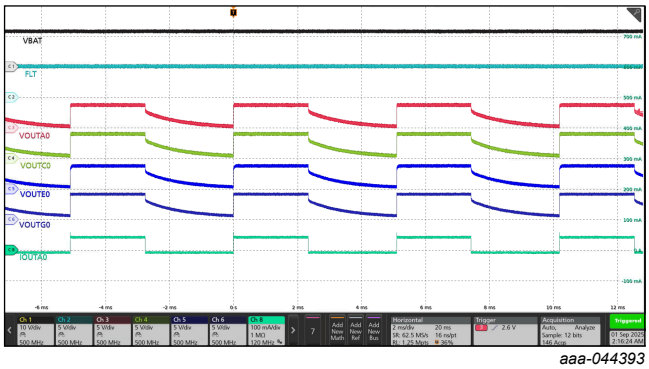

Fig. 15. PWM dimming at 200 Hz

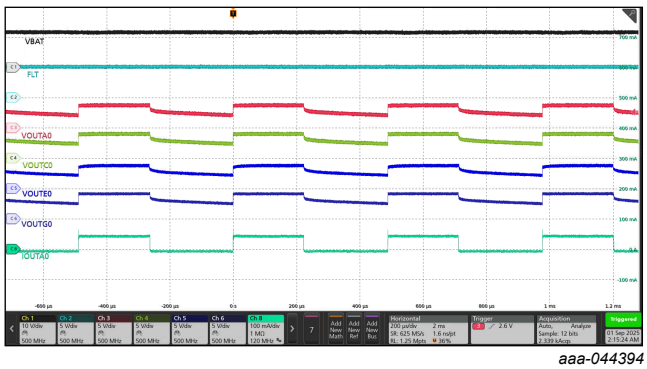

Fig. 16. PWM dimming at 2000 Hz

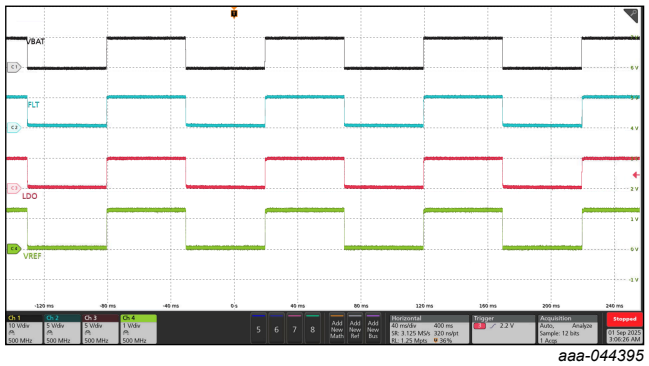

Fig. 17. Vbat start-up and shutdown

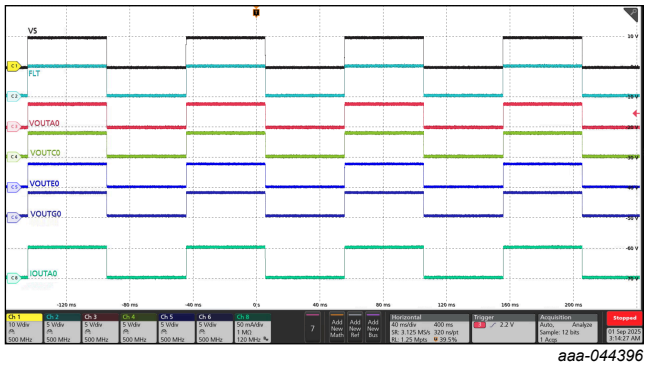

Fig. 18. Vs start-up and shutdown

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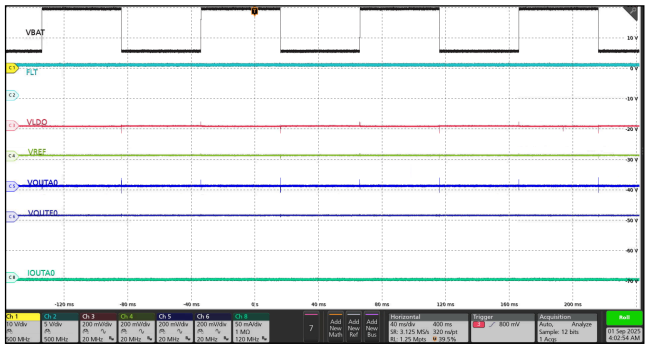
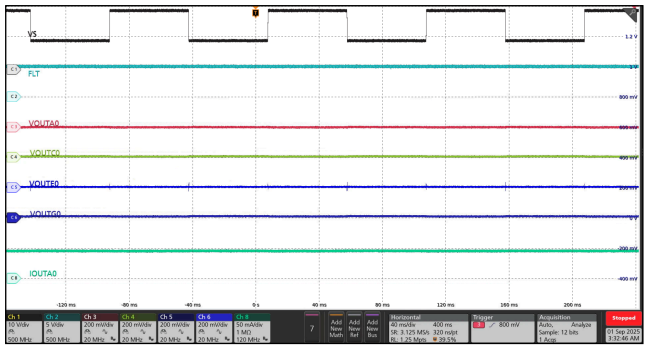


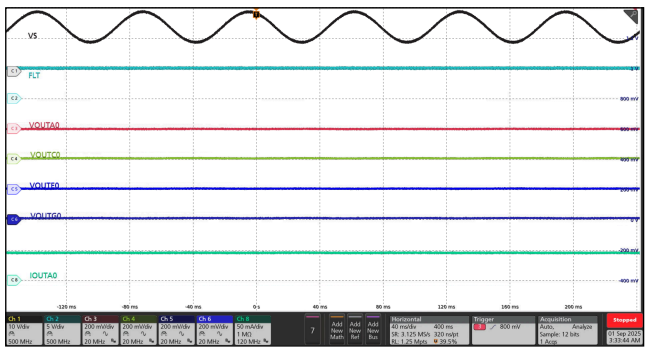
aaa-044397

Fig. 19. Vbat transient



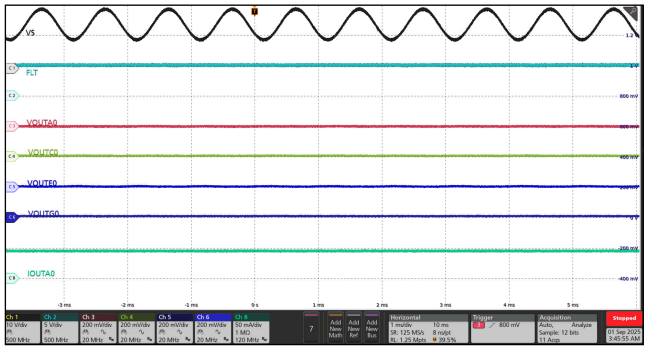
aaa-044398

Fig. 20. Vs transient



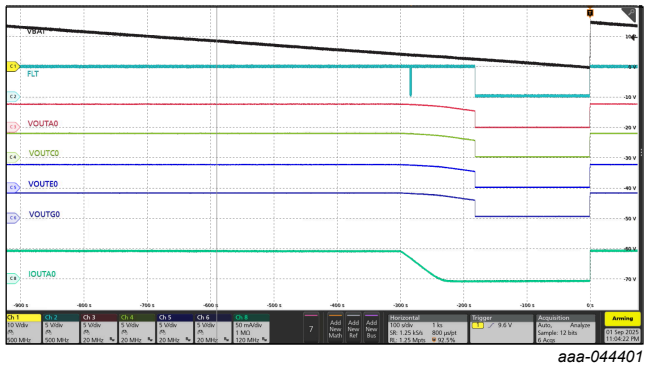
aaa-044399

Fig. 21. Super-imposed alternating voltage 15 Hz



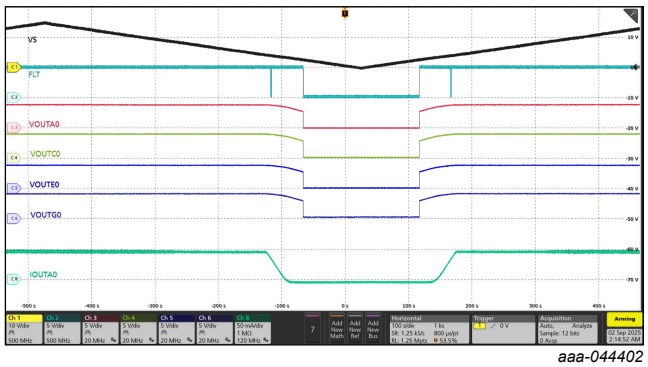
aaa-044400

Fig. 22. Super-imposed alternating voltage 1 kHz



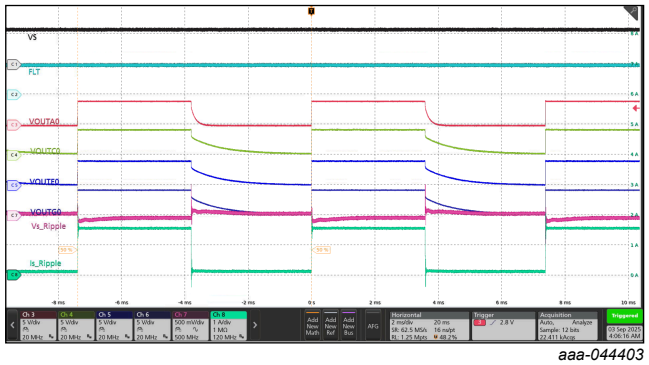
aaa-044401

Fig. 23. Slow decrease and quick increase of supply voltage



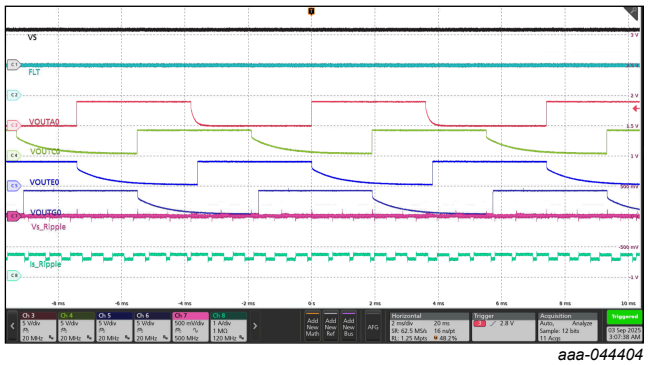
aaa-044402

Fig. 24. Slow decrease and slow increase of supply voltage



aaa-044403

Fig. 25. Phase shift disable



aaa-044404

Fig. 26. Phase shift enable

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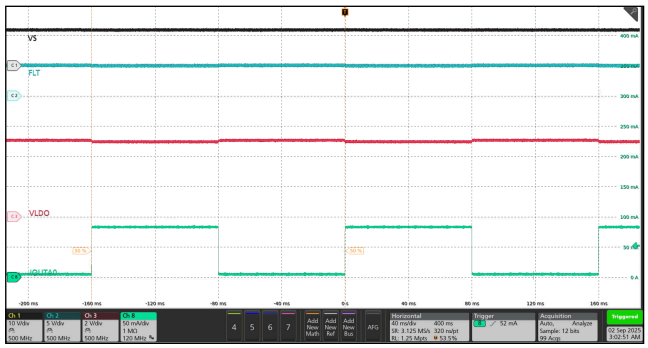
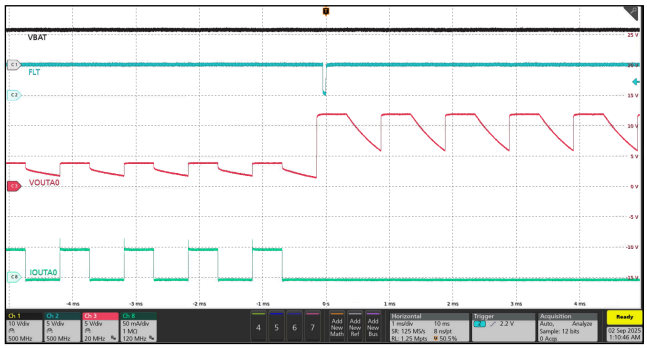


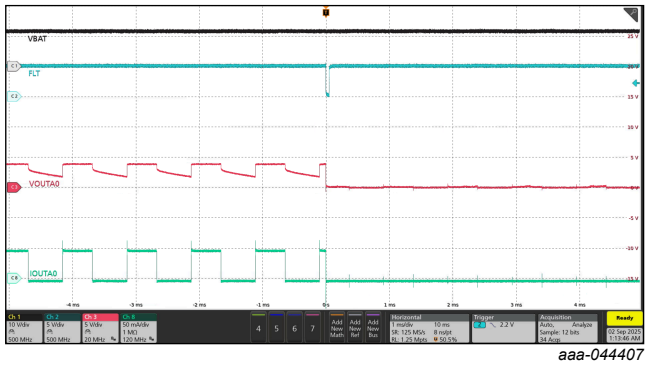
aaa-044405

Fig. 27. LDO output load transient



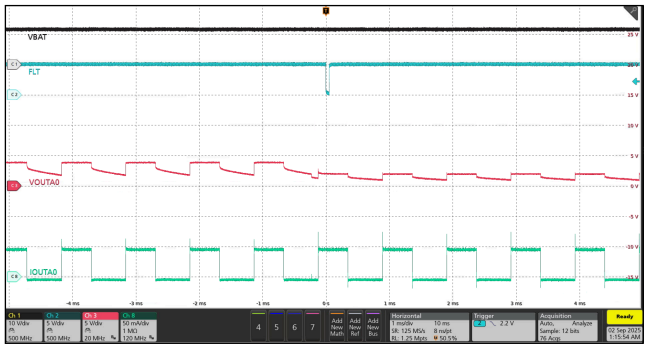
aaa-044406

Fig. 28. LED open-circuit detection in NORMAL state



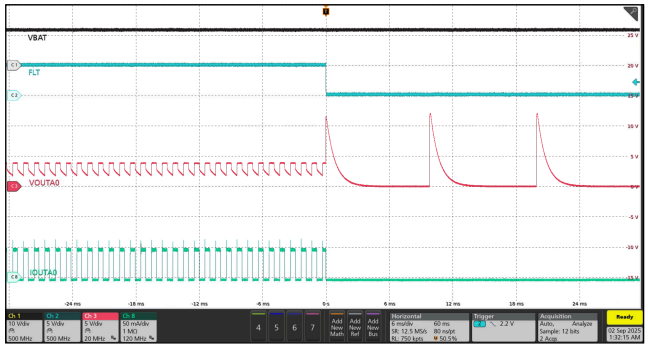
aaa-044407

Fig. 29. LED short-circuit detection in NORMAL state



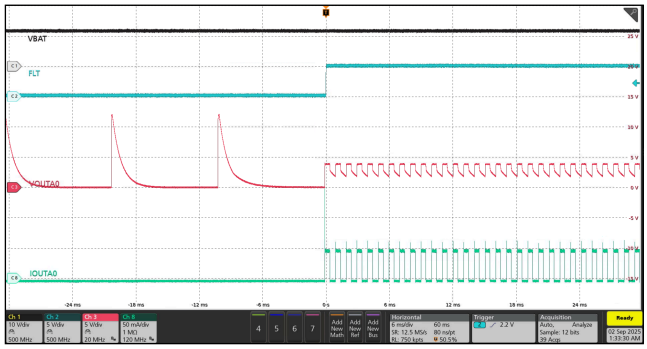
aaa-044408

Fig. 30. Single-LED short circuit detection in NORMAL state



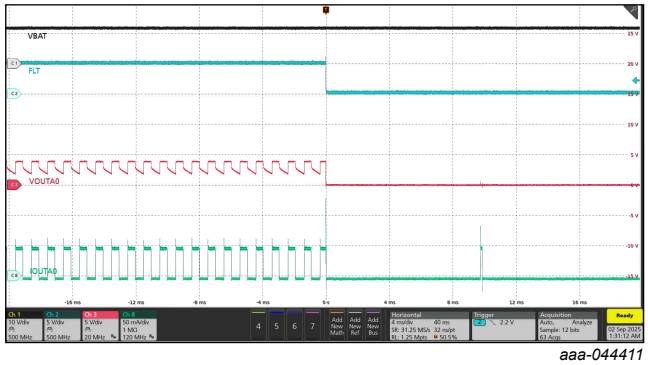
aaa-044409

Fig. 31. LED open-circuit detection in Fail-Safe state



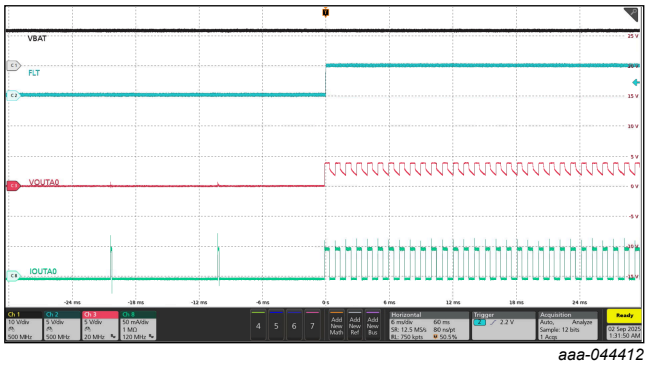
aaa-044410

Fig. 32. LED open-circuit recovery in Fail-Safe state



aaa-044411

Fig. 33. LED short-circuit detection in Fail-Safe state



aaa-044412

Fig. 34. LED short-circuit recovery in Fail-Safe state

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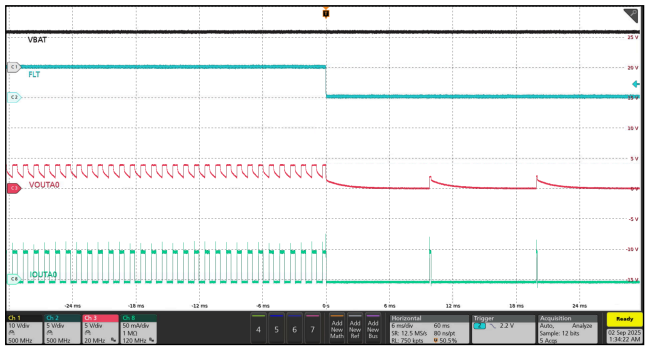
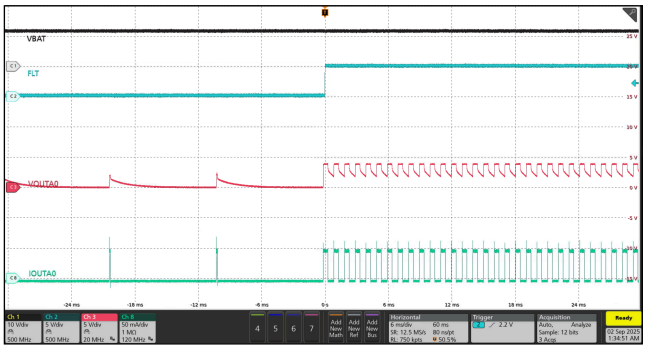


aaa-044413

Fig. 35. Single-LED short-circuit detection in Fail-Safe state



aaa-044414

Fig. 36. Single-LED short-circuit recovery in Fail-Safe state

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15. Detailed description

15.1. Overview

The NEX1324X-Q100 is an automotive 24-channel LED driver equipped with a UART interface to meet the growing demand for individual control of each LED string. Each channel supports both analog dimming and pulse-width modulation (PWM) dimming, configurable via the UART. The internal MTP (Multi-time Programming memory) enables users to set configurations in the event of communication loss, ensuring compliance with system-level function safety requirements.

The integrated UART interface is compliant with physical layer transceiver such as CAN or LIN transceivers. It can support off board communication with the transition of CAN or LIN transceivers.

To optimize the total system cost, two interface versions are provided. NEX13240-Q100 is the UART version, and NEX13241-Q100 integrates a CAN transceiver to save the external CAN transceiver. For more details, refer to Fig. 37 and Fig. 38.

Each output channel serves as a constant current source, allowing for individually programmable current outputs and PWM duty cycles. The device includes various diagnostic features, such as LED open-circuit, short-circuit, and single-LED short-circuit detection. Additionally, the on-chip analog-to-digital converter (ADC) enables real-time monitoring of output conditions.

To enhance robustness, NEX1324X-Q100 integrates Fail-Safe state machine that automatically switches to Fail-Safe states in case of communication loss, such as MCU failure. Users can program Fail-Safe settings using the MTP, allowing for different configurations in the event of output failure, such as one-fails-all-fail or one-fails-others-on. Each channel can be independently programmed to either remain on or off during Fail-Safe states.

The Fail-Safe state machine also permits the system to operate with pre-programmed MTP settings without the presence of a controller, enabling stand-alone operation. The microcontroller can access each device through the UART interface, allowing full control over the device and LEDs by setting and reading back registers. All MTPs are pre-programmed with default values, and Nexperia recommends that users program the MTP at the end of the production line for application-specific settings and Fail-Safe configurations.

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15.2. Function block diagram

The NEX1324X-Q100 function block diagrams are shown below:

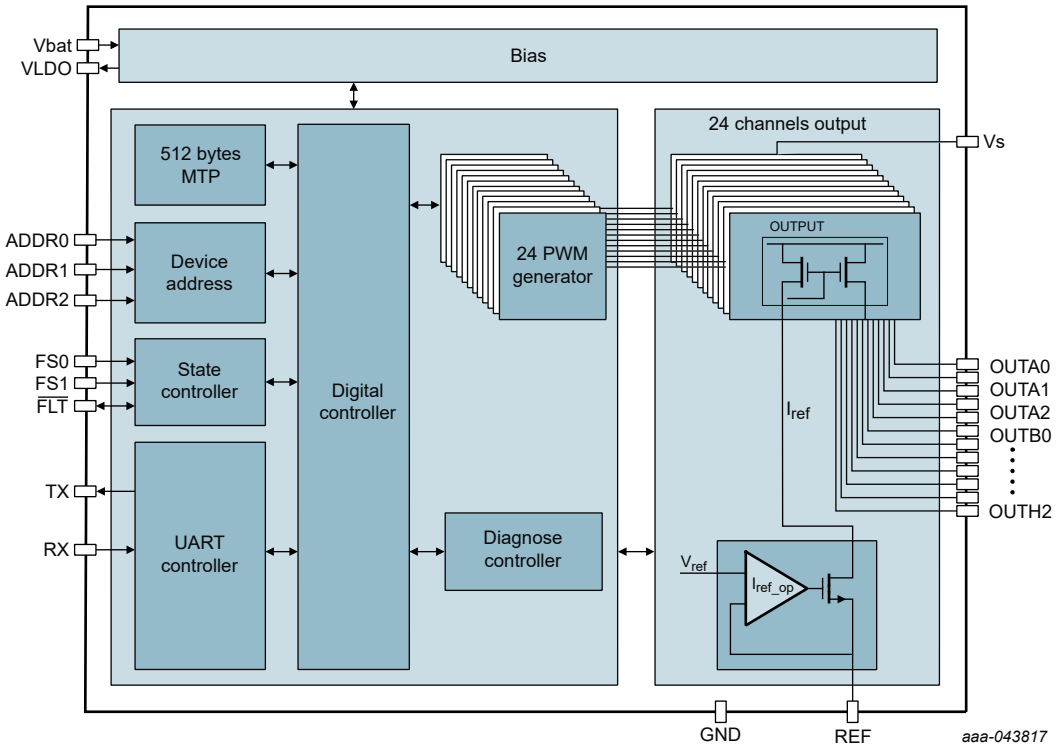

Fig. 37. NEX13240-Q100 function block diagram

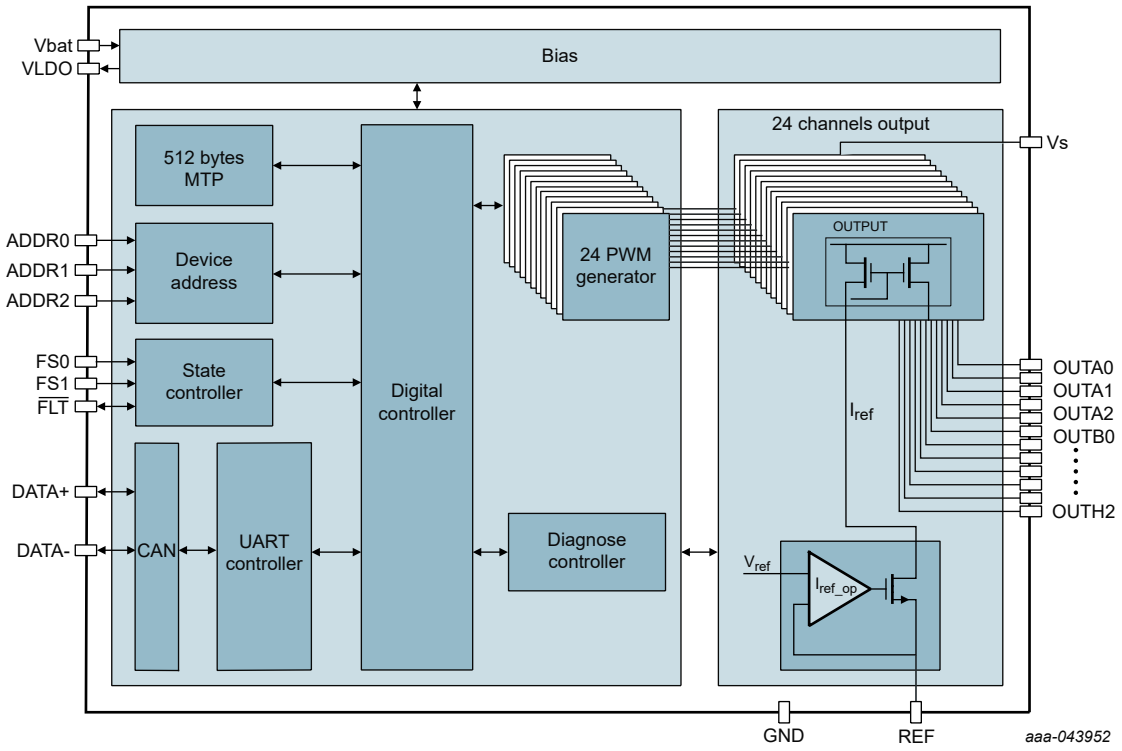

Fig. 38. NEX13241-Q100 function block diagram

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15.3. Feature description

15.3.1. Device bias and power

Power supply (Vbat)

NEX1324X-Q100 is AECQ-100 qualified for automotive applications. The power input to the device through Vbat pin can be low to 4.5 V and up to 40 V for automotive battery directly powered systems. All the internal analog and digital circuits except for the current output channels are powered by Vbat.

5 V Low-Drop-Out linear regulator (VLDO)

NEX1324X-Q100 has an integrated low-drop-out linear regulator to provide power supply to external CAN transceivers. The internal LDO powered by input voltage V_{Vbat} provides a stable 5 V output with up to 80 mA constant current capability. Nexperia recommends a ceramic capacitor from 1 µF to 10 µF on the VLDO pin. The LDO has an internal current limit I_{VLDO_limit} for protection and soft start. The capacitor charging time must be considered to total start-up time because the device is held in POR state if the capacitor voltage is not charged to above UVLO threshold.

Undervoltage Lockout (UVLO) and Power-On-Reset (POR)

NEX1324X-Q100 uses UVLO and POR circuitry to clear its internal registers upon power up and to reset registers with its default values. NEX1324X-Q100 has internal UVLO circuits so that when either input voltage V_{Vbat} or LDO output voltage V_{VLDO} is lower than its UVLO threshold, POR is triggered. In POR state, the device resets digital core and all registers to default value. FLAG_POR and FLAG_ERR register are set to 1 for each POR cycle to indicate the POR history. Before both powers are above UVLO thresholds, NEX1324X-Q100 stays in POR state with all outputs off and $\overline{FLT}$ pin pulled down. Once both power supplies are above UVLO threshold, the device enters INIT mode for initialization releasing $\overline{FLT}$ pin pull-down.

A programmable timer starts counting in INIT state, the timer length can be set by MTP register INITTIMER. When the timer is completed, the device switches to NORMAL state. In INIT state, setting CLR_POR to 1 clears FLAG_POR, disables the timer, and sets the device to NORMAL state.

Upon powering up, NEX1324X-Q100 automatically loads all settings stored in MTP to correlated registers and sets the other registers to default value which do not have correlated MTP. All channels are powered up off-state by default to avoid unwanted blinking. Writing 1 to REGDEFAULT manually loads MTP setting to the correlated registers and set the other registers to default value. After REGDEFAULT is set, the FLAG_POR is cleared to 0.

Writing 1 to CLR_POR also resets the FLAG_POR register to 0. Nexperia recommends setting CLR_REG to 1 to clear the internal registers every time after POR. The REGDEFAULT automatically resets to 0.

Power supply (Vs)

NEX1324X-Q100 has an additional Vs input pin for powering all 24 high-side current output channels. The V_{Vs} can be low to 3.8 V and up to 20 V for either automotive battery directly powered systems or an external DC-DC converter output. An external DC-DC converter can provide a regulated voltage for required LED output forward voltage from wide automotive battery voltage range.

NEX1324X-Q100 has an internal undervoltage detection circuit for Vs input. When the Vs input voltage is lower than undervoltage threshold, $V_{Vs\_th\_fall}$, all 24 current output channels are disabled with $\overline{FLT}$ pin constantly pulled low and register flags set to 1 including FLAG_ERR bit and FLAG_VSUV bit. Table 19 shows the detailed fault behavior in NORMAL state.

Programmable low-supply warning

NEX1324X-Q100 uses its internal ADC to monitor supply voltage V_{Vs}. If the V_{Vs} is below allowable working threshold, the output voltage can be insufficient to keep the LED operating with the desired brightness output as expected. The V_{Vs} is automatically compared with the threshold set by register LOWVSTH.

When the V_{Vs} is below the threshold, the device sets the warning flag register FLAG_LOWVS and FLAG_ERR to 1 in the status register. CLRFAULT can clear the FLAG_LOWVS as well as other fault registers. Low-supply warning will clear LED open and single-LED short faults, the FLAG_OPENOUTXn and FLAG_SLSOUTXn can be cleared by CLR_ERR.

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In addition, the LED open circuit and single-LED short-circuit detection is disabled if the V_{Vs} is below threshold to avoid the LED open circuit and to prevent the single-LED short-circuit fault from being mis-triggered. The 5-bit register LOWVSTH has a total of 32 options covering from 4 V to 35 V as shown in Table 11.

Table 11. Low supply warning threshold setting

	Calculation formula
LOWVSTH Voltage (V)	LOWVSTH [4:0] + 4 V

15.3.2. Constant current output

Constant current output reference current with external resistor (R_{REF})

NEX1324X-Q100 must have an external resistor R_{REF} to set the internal current reference I_{REF} as shown in below Fig. 39.

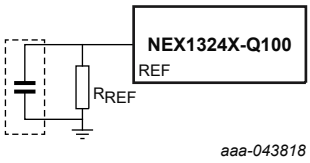

Fig. 39. Output current setting

The internal current reference, I_{full_range}, is generated based on the I_{REF} multiplied by factor K_{REF} to provide the full range current reference for each OUTx channel. The K_{REF} is programmable by 2-bit register REFRANGE with four different options. Use equation (1) to calculate the I_{full_range}:

$$I_{full\_range} = \frac{V_{REF}}{R_{REF}} \cdot K_{REF} \quad (1)$$

Where V_{REF} = 1.235 V, K_{REF} = 64, 128, 256 or 512 (default).

Table 12. Reference current range setting

Reference	K_{REF}	Full range current (mA)			
		R_{REF} = 6.34 kΩ	R_{REF} = 8.45 kΩ	R_{REF} = 12.7 kΩ	R_{REF} = 31.6 kΩ
11b	512	100	75	50	20
10b	256	50	37.5	25	10
01b	128	25	18.75	12.5	5
00b	64	12.5	9.375	6.25	2.5

Nexperia recommends placing the R_{REF} resistor as close as possible to the REF pin with an up to 2.2 nF ceramic capacitor in parallel to improve noise immunity. Nexperia recommends a 1 nF ceramic capacitor in parallel with R_{REF}.

64-step programmable high-side constant-current output

NEX1324X-Q100 has 24-channels of high-side current sources. Each channel has its own enable configuration register ENOUTXn. Setting ENOUTXn to 1 enables the channel output, clearing the register to 0 disables the channel output. To completely turn off the channel current, user can clear channel enable bit ENOUTXn to 0. Upon powering up, ENOUTXn is automatically reset to 0 to prevent unwanted blinking.

Each OUTXn channel supports individual 64-step programmable current setting, also known as Dot Correction (DC). The DC feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on external visual system to further save binning cost. The 6-bit register IOUTXn sets the current independently, where n is the channel number from 0 to 23. The OUTXn current can be calculated with equation (2):

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$$I_{OUTXn} = \frac{IOUTXn + 1}{64} \times I_{full\_range} \quad (2)$$

Where:

- IOUTXn is programmable from 0 to 63.
- X is from A to H.
- n is from 0 to 2 for different output channel.
- I_{full_range} can be calculated with equation (1).

15.3.3. PWM dimming

NEX1324X-Q100 integrates independent 12-bit PWM generators for each OUTXn channel. The integrated PWM generator turns the current output for each OUTXn channel on and off. The average current of each OUTXn can be adjusted by PWM duty cycle independently, therefore, to control the brightness for LEDs in each channel.

PWM dimming frequency

The frequency for PWM dimming is programmable by 4-bit register PWMFREQ and register PWMSLOW with 16 options covering from 200 Hz to 23.4 kHz. Select the frequency for PWM dimming based on the minimum brightness requirement in application. NEX1324X-Q100 supports down to 1 µs minimum pulse current for all 24-channel outputs.

Table 13. PWM frequency setting

PWM frequency setting PWMFREQ	PWM cycle frequency
0	200
1	250
2	300
3	350
4	400
5	500
6	600
7	750
8	1000
9	1200
10	2000
11	4000
12	5800
13	7800
14	11700
15	23400

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Blanking time

Since NEX1324X-Q100 supports PWM control for adjusting LED brightness, the voltage on OUTXn is like a pulse waveform. The output voltage and current ramp up to the target value in a certain period after the channel is turned on depending on the value of capacitor on the OUTXn pin. The ramping up period is proportional to the capacitance value of the capacitor.

To prevent the output voltage of each OUTXn being measured in the ramping up transient period, NEX1324X-Q100 integrates a t_{BLANK} timer which is programmable by a 4-bit register BLANK to set up the blanking time for all OUTXn. The device does not start the OUTXn diagnostics and ADC measurement until the t_{BLANK} timer is overflown. The t_{BLANK} timer is programmable from 20 µs to 4 ms as described in Table 14. Nexperia recommends setting the t_{BLANK} less than the PWM dimming period, which is programmable by PWMFREQ register, otherwise the OUTXn diagnostics and ADC measurement only operates properly when PWM duty cycle is set to 100%.

Table 14. BLANK time setting

	BLANK time															
Binary code	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
t_{BLANK} (µs)	100	20	30	50	80	150	200	300	500	800	1000	1200	1500	2000	3000	4000

Phase shift PWM dimming

The phase shift PWM dimming mode is enabled by setting PSEN to 1. In phase shift PWM dimming mode, every three current output channels are formed as one group, so a total of eight current output groups are turned on and off at PWM dimming frequency set by PWMFREQ register with a delay configured by PSθ. The detailed group information and shift delay are listed in Table 15.

Table 15. Groups and shift delay

Group	Outputs	CONF_PSθ	Description
Group A	OUTA0, OUTA1, OUTA2	0	delay time is 1/8 of $1/F_{PWM}$
Group B	OUTB0, OUTB1, OUTB2	1	delay time is 1/12 of $1/F_{PWM}$
Group C	OUTC0, OUTC1, OUTC2	2	delay time is 1/16 of $1/F_{PWM}$
Group D	OUTD0, OUTD1, OUTD2	3	delay time is 1/24 of $1/F_{PWM}$
Group E	OUTE0, OUTE1, OUTE2	-	-
Group F	OUTF0, OUTF1, OUTF2	-	-
Group G	OUTG0, OUTG1, OUTG2	-	-
Group H	OUTH0, OUTH1, OUTH2	-	-

Linear brightness control

When register EXPEN is set to 0, the MSB 8 bits of 12-bit binary input to PWM generator are directly copied from 8-bit register PWMOUTXn, and the LSB 4 bits are directly copied from 4-bit register PWMLOWOUTXn. The PWM output duty cycle can be calculated with equation (3). The PWM output duty cycle is linearly controlled by the register PWMOUTXn and PWMLOWOUTXn, which provides linear brightness control to each channel output. When PWMOUTXn is 00h, and PWMLOWOUTXn is 0h, the duty cycle is 0% exceptionally.

$$D_{OUTXn} = \frac{16 \times PWMOUTXn + PWMLOWOUTXn + 1}{4096} \times 100\% \quad (3)$$

Where:

PWMOUTXn is decimal number from 0 to 255.
PWMLOWOUTXn is decimal number from 0 to 15.
X is from A to H.
n is from 0 to 2.

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Since 12-bit PWM duty cycles require 2 bytes of write operation to update the completed data, the output PWM duty cycle is not changed in between of the two bytes data transmission. NEX1324X-Q100 only updates the PWM duty cycle of any output when its high 8-bit PWMOUTn is written. When very fast brightness change is needed, such as fade-in and fade-out effects, it is essential to change the PWM duty cycles of all channels simultaneously.

To reduce the data transmission for large quantity of the LED pixel control, 8-bit PWM duty cyle resolution can be adopted by writing 0 to 12-bit in DIM register. The master only needs to update high 8-bit PWMOUTXn register to change the brightness of target output channel. The low 4-bit registers PWMLOWOUTXn are ignored. The PWM duty-cycle calculation is shown as equation (4). When PWMOUTXn is 00h, the duty cycle is 0% exceptionally.

$$D_{OUTXn} = \frac{PWMOUTXn + 1}{256} \times 100\,\% \quad (4)$$

Setting SHAREPWM to 1 enables all channels using the PWM duty cycle setting of channels 0 to reduce communication latency.

Exponential brightness control

NEX1324X-Q100 can generate PWM duty-cycle outputs that follow an exponential curve. When the EXPEN register is set to 1, the integrated conversion circuit provides a one-to-one conversion from the 8-bit register PWMOUTXn to a 12-bit binary code that follows an exponential increment, as illustrated in Fig. 40. When exponential control path is selected, the PWMLOWOUTXn data is neglected. By using the exponential brightness control, LED brightness changes by one LSB is invisible to human eyes especially at low brightness range.

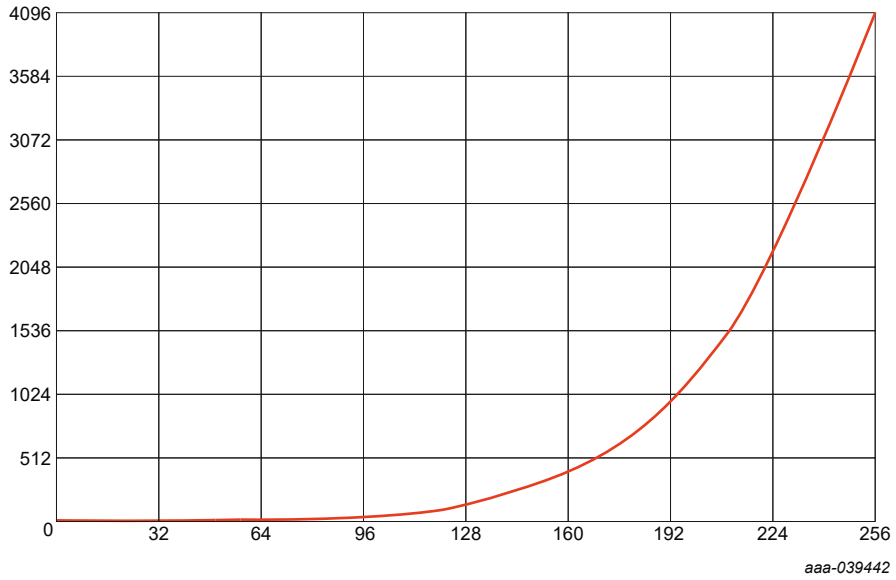

Fig. 40. PWM duty cycle versus 8-bit code for exponential dimming

During power-up or in Fail-Safe state, the registers EXPEN, and PWMFREQ are automatically reset to their default values stored in their corresponding MTP. Both PWMOUTXn and PWMLOWOUTXn are reset to 00h during power up but load their MTP content in Fail-Safe state.

15.3.4. Fail-Safe state operation

In Fail-Safe state, the FS pin can be used as control signal to turn on or turn off the corresponding channel. Each current output channel has its own register, FSOUTXn to set the mapping to FS0 or FS1. When FSOUTXn is set to 0, the corresponding current output channel is controlled by FS0 input, otherwise it is controlled by FS1 input.

NEX1324X-Q100 supports independent channel brightness control through the UART interface. The brightness of each channel is adjustable according to its DC current register I_{OUTXn}, PWM duty cycle register PWMOUTXn, PWMLOWOUTXn and channel enable register ENOUTXn setting. The brightness of each channel reflects its register setting value immediately after register is successfully updated through the differential data interface by the master unit.

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However, the master unit will lose control for all current channels if the UART communication fails between master unit and NEX1324X-Q100. For example, the interface cable broke by accident. Therefore, the brightness for all output channels of NEX1324X-Q100 is stuck and the ON and OFF control for all output channels are missing too. To keep the basic ON and OFF control for each output channel, NEX1324X-Q100 provides a Fail-Safe state when the communication to master is lost. For detailed description for Fail-Safe state entering and quitting criteria, refer to Section 15.4.

When NEX1324X-Q100 is entering Fail-Safe state, all the registers are set to default value or reloaded from MTP, including IOUTXn, PWMOUTXn and ENOUTXn. The pre-programmed settings in the MTP are loaded and the corresponding registers are reset to the default values.

During the MTP loading process, all the PWM output channels are disabled, and the channels' faults detected in the NORMAL state are cleared. NEX1324X-Q100 provides two hardware input pins, FS0 and FS1 to turn on or off corresponding current output channels in Fail-Safe state. Each current output channel has its own register, FSOUTXn to set the mapping to FS0 or FS1. When FSOUTXn is set to 0, the corresponding current output channel is controlled by FS0 input, otherwise it is controlled by FS1 input.

- If the voltage of FSx input is higher than its high threshold, $V_{IH(IO)}$, all current output channels mapped to FSx input are turned on.
- When the voltage of FSx input drops below low threshold, $V_{IL(IO)}$, all current out channels mapped to FSx input are turned off.

The flag register FLAG_EXTFSx shows the FSx input level at real-time. If FSx pin input voltage is logic high, the FLAG_EXTFSx is set to 1. All FSOUTXn registers load their corresponding MTP data when NEX1324X-Q100 enters Fail-Safe state.

The Fail-Safe state also allows NEX1324X-Q100 to operate as a standalone device without master controlling in the system. The ERR pin is used as a fault indicator to achieve one-fails-all-fail or one-fails-others-on diagnostics requirement. When low quiescent current in fault mode is required, the device must be set as one-fails-all-fail. In this case, if a fault is triggered, the device goes into low current fault mode.

15.3.5. 8-bit ADC

NEX1324X-Q100 has integrated a successive-approximation-register (SAR) ADC for diagnostics. It routinely monitors supply voltage if the ADC is idle and uses this voltage to detect V_{Vs} undervoltage and low V_{Vs} warning fault.

To manually read the voltage of an ADC channel as listed in Table 16, users must write the 5-bit register ADCCH to select channels. Once ADCCH register is written, the one-time ADC conversion starts and clears FLAG_ADCDONE register. If the ADC conversion is completed, the ADC result is available in 8-bit register ADC_OUT and sets FLAG_ADCDONE to 1. Reading the ADC_OUT register also clears FLAG_ADCDONE, and the FLAG_ADCDONE is set to 0 after reading completion.

Since NEX1324X-Q100 supports PWM control for adjusting LED brightness, the voltage on OUTXn is like a pulse waveform.

- When the current output is enabled by setting ENCHXn to 1, the ADC measures the voltage on assigned OUTXn after the channel is turned on with t_{diag_pulse} delay time, which is programmable by 4-bit register BLANK.
- When the channel is disabled by setting ENCHXn to 0, the ADC samples the voltage on assigned OUTXn at off state. The analog value can be calculated based on the read back binary code with equation (5) and Table 16.

$$Analog Value = a + K \times ADC\_OUT \quad (5)$$

Where ADC_OUT is the decimal number from 0 to 255.

In ADC auto-scan mode, If MAXOUT channel is selected by writing 06h to ADCCH, the maximum voltage of OUTA0 to OUTH2 is recorded into ADC_OUT register. The maximum channel output voltage is available after at least one output PWM cycle is completed.

Based on the measured maximum output voltage and supply voltage, microcontroller can regulate supply voltage from previous power stage to minimize the power consumption on the NEX1324X-Q100. Basically, a microcontroller needs to program the output voltage of previous power stage to be just higher than the measured maximum channel output voltage plus the required dropout voltage V_{OUT_drop} of NEX1324X-Q100. In this way, NEX1324X-Q100 can achieve minimum power consumption, and overall power efficiency is optimized.

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Table 16. ADC channel definition

Channel	ADCCH	Name	ADC calculation parameter (a)	ADC calculation parameter (k)	Comment
0	00h	REF	0.007 V	0.0101 V/LSB	reference voltage
1	01h	VS	0.1346 V	0.1608 V/LSB	supply voltage
2	02h	VLDO	0.0465 V	0.022 V/LSB	5 V VLDO output voltage
3	03h	TEMPSNS	–270.312 °C	2.688 °C/LSB	internal temperature sensor
4	04h	IREF	0.9969 µA	0.9969 µA/LSB	reference current
5	05h	VBAT	0.1346 V	0.1608 V/LSB	Vbat pin voltage
6	06h	MAXOUT	0.0673 V	0.0804 V/LSB	maximum channel output voltage
7	07h	reserved			
8	08h	OUTA0	0.0673 V	0.0804 V/LSB	output voltage channel A0
9	09h	OUTA1			output voltage channel A1
10	0Ah	OUTA2			output voltage channel A2
11	0Bh	OUTB0			output voltage channel B0
12	0Ch	OUTB1			output voltage channel B1
13	0Dh	OUTB2			output voltage channel B2
14	0Eh	OUTC0			output voltage channel C0
15	0Fh	OUTC1			output voltage channel C1
16	10h	OUTC2			output voltage channel C2
17	11h	OUTD0			output voltage channel D0
18	12h	OUTD1			output voltage channel D1
19	13h	OUTD2			output voltage channel D2
20	14h	OUTE0			output voltage channel E0
21	15h	OUTE1			output voltage channel E1
22	16h	OUTE2			output voltage channel E2
23	17h	OUTF0			output voltage channel F0
24	18h	OUTF1			output voltage channel F1
25	19h	OUTF2			output voltage channel F2
26	1Ah	OUTG0			output voltage channel G0
27	1Bh	OUTG1			output voltage channel G1
28	1Ch	OUTG2			output voltage channel G2
29	1Dh	OUTH0			output voltage channel H0
30	1Eh	OUTH1			output voltage channel H1
31	1Fh	OUTH2			output voltage channel H2

15.3.5.1. Minimum on-time for ADC measurement

Since NEX1324X-Q100 supports PWM control for adjusting LED brightness, the voltage on OUTXn is like a pulse waveform. When the current output is enabled by setting ENOUTXn to 1, the ADC measures the voltage on assigned OUTXn after the output is turned on with t_{BLANK}delay time, which is programmable by 4-bit register BLANK. The minimum current output pulse on assigned OUTXn must be longer than $t_{BLANK} + 3 \times t_{CONV}$ to make sure the correct measured result for OUTXn at ON state. When the output is disabled by setting ENOUTXn to 0, the ADC samples the voltage on assigned OUTXn at OFF state.

Nexperia recommends setting 100% duty cycle on assigned OUTXn for ADC measurement by writing FFh to PWMOUTXn and 0Fh to PWMLOWOUTXn register when the PWM dimming period t_{DIM_cycle} has to be less than $t_{BLANK} + 3 \times t_{CONV}$.

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15.3.5.2. ADC auto scan and ADC error

ADC auto scan

In ADC auto scan mode, If the MAXOUT channel is selected by writing 06h to ADCCHSEL, the maximum voltage of OUTXn is recorded into ADC_OUT register. The maximum channel output voltage is available after at least nine output PWM cycles are completed.

The ADC measures every three outputs as one group when the group is turned on and moved to measure the next group in next PWM dimming cycle until all eight groups are completed no matter in PWM dimming mode or phase shift PWM dimming mode.

The device sets FLAG_ADCDONE to 1 and stops ADC auto scan after the measurements for all eight groups are done. The FLAG_ADCDONE is cleared to 0 by reading the ADC_OUT, and ADC auto scan restarts again if the data of ADCCHSEL is still 06h. FLAG_ADCDONE is also cleared to 0 by writing ADCCHSEL register, and ADC restarts after FLAG_ADCDONE is cleared. The minimum current pulse for each output must be longer than t_{BLANK} + 3 × t_{CONV} in auto scan mode. The channel is skipped if it is disabled in auto scan mode.

Based on the measured maximum output voltage and supply voltage, the microcontroller can regulate supply voltage from previous power stage to minimize the power consumption on the NEX1324X-Q100. Basically, the microcontroller must program the output voltage of previous power stage to be just higher than the measured maximum channel output voltage plus the required dropout voltage V_{OUT_drop} of the NEX1324X-Q100. In this way, NEX1324X-Q100 takes minimum power consumption, and overall power efficiency is optimized.

ADC error

NEX1324X-Q100 integrates a digital comparator to measure the PWM dimming period t_{DIM_cycle} and t_{BLANK}+ 3 × t_{CONV} at real time when ADC is started by writing ADCCHSEL register or reading ADC_OUT register. The device stops the ADC measurement and sets the FLAG_ADCERR register to 1 if the t_{DIM_cycle} is measured less than t_{BLANK} + 3 × t_{CONV} time. The FLAG_ADCERR register is cleared to 0 by writing 1 to the CLRFAULT register.

15.3.6. Diagnostic and protection in NORMAL state

NEX1324X-Q100 has a full diagnostic coverage for supply voltage, current output, and junction temperature.

In NORMAL state, the device detects all failures and reports the status out through the $\overline{FLT}$ pin or FLAG registers, without any actions taken by the device except Vbat UVLO, V_{Vs} undervoltage and overtemperature protection. The master controller must handle all fault actions, for example, retry several times and shut down the outputs if the error still exists.

V_{Vbat} and V_{VLDO} undervoltage lockout diagnostics in NORMAL state

When V_{Vbat} or V_{VLDO} drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1. The master controller can write 1 to register CLR_POR to clear the FLAG_POR, write 1 to CLRFAULT to clear FLAG_ERR, and the CLR_POR, CLRFAULT bit automatically returns to 0.

Low-supply warning diagnostics in NORMAL state

NEX1324X-Q100 continuously monitors the V_{Vs} and compares the results with internal threshold $V_{LOWVSTH}$ set by LOWVSTH for low-supply voltage warning. If the supply voltage is lower than threshold, the device pulls $\overline{FLT}$ pin down with one pulsed current sink for 50 µs to report the fault and set flag registers including FLAG_LOWVS and FLAG_ERR to 1. The fault is latched in flag registers.

- When the V_{Vs} rises above low-supply warning threshold, the master controller must write 1 to register CLRFAULT to clear FLAG_LOWVS and FLAG_ERR. The CLRFAULT bit automatically returns to 0. The low-supply warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection.
- When the voltage applied on Vs pin is higher than the threshold $V_{LOWVSTH}$, NEX1324X-Q100 enables LED open-circuit and single-LED short-circuit diagnosis. When V_{Vs} is lower than the threshold $V_{LOWVSTH}$, the device disables LED-open-circuit detection and single-LED short-circuit diagnosis.

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Since when V_{Vs} drops below the maximum total LED forward voltage plus required V_{OUT_drop} at required current, NEX1324X-Q100 is not able to deliver sufficient current output. The device pulls the voltage of each output channel as close as possible to the Vs. In this condition, the LED open-circuit fault or single-LED short-circuit fault can be detected and reported mistakenly. Setting the low-supply warning threshold high enough can prevent the LED open-circuit and single LED short-circuit fault being detected when V_{Vs} drops to low. The $V_{LOWVSTH}$ is programmable from 4 V to 35 V at 1-V interval.

Supply undervoltage diagnostics in NORMAL state

NEX1324X-Q100 provides an internal analog comparator to monitor the V_{Vs} for undervoltage protection. If the V_{Vs} falls below the internal threshold, $V_{Vs\_th\_fall}$, the device pulls the $\overline{FLT}$ pin low with constant current sink to report the fault and set flag registers including FLAG_VSUV and FLAG_ERR to 1. The supply undervoltage detection is used to disable all current output.

When the voltage applied on the Vs pin is higher than the threshold $V_{Vs\_th\_rise}$, NEX1324X-Q100 enables all current outputs. When V_{Vs} is lower than the threshold $V_{Vs\_th\_fall}$, the device disables every output to avoid the unwanted LED flickering or output fault triggered improperly.

The fault is latched in flag registers. When the supply voltage rises above $V_{Vs\_th\_rise}$, the master controller must write register CLRFAULT to 1 to clears FLAG_VSUV and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Reference diagnostics in NORMAL state

NEX1324X-Q100 integrates diagnostics for REF resistor open and short fault in NORMAL state. The device monitors the reference current I_{REF} set by external resistor R_{REF}. Use equation (6) to calculate the I_{REF}.

$$I_{REF} = \frac{V_{REF}}{R_{REF}} \quad (6)$$

V_{REF} typically is 1.235 V.

If the current output from REF pin I_{REF} is lower than $I_{REF\_OPEN\_th}$, the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin V_{REF} is lower than $V_{REF\_SHORT\_th}$. The device pulls the $\overline{FLT}$ pin down with constant current sink and sets flag registers including FLAG_REF and FLAG_ERR to 1.

The fault is latched in flag registers. After the REF pin I_{REF} and $V_{REF\_SHORT\_th}$ recover to normal, the device releases $\overline{FLT}$ pin pull-down automatically and the master controller must send CLRFAULT to clears FLAG_REF and FLAG_ERR. CLRFAULT automatically returns to 0.

In NORMAL state, the device does not perform any actions automatically when reference resistor fault is detected. However, the output may not work properly, and the output current may be operating at high current level. Nexperia recommends for master controller to shut down the device outputs and report error to upper level control system such as body control module (BCM).

Pre-thermal warning in NORMAL state

NEX1324X-Q100 has pre-thermal warning at typical 135 °C. When the junction temperature, T_j, of NEX1324X-Q100 rises above pre-thermal warning threshold, the device reports pre-thermal warning, pulls $\overline{FLT}$ pin with pulsed current sink for 50 µs and sets the flag registers including FLAG_PRETSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature of NEX1324X-Q100 falls below pre-thermal warning threshold, the master controller must write 1 to CLRFAULT register to clears FLAG_PRETSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0. When more accurate thermal measurement on LED unit is required, one current output channel can be sacrificed to provide current bias to external thermal resistor such as PTC or NTC.

The voltage of external thermal resistor can be measured by integrated ADC to acquire the temperature information of the thermal resistor located area. The master controller can determine actions based on the acquired temperature information to turn off or reduce current output.

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Overtemperature protection in NORMAL state

NEX1324X-Q100 has overtemperature protection at T_{TSD1}, typical 175 °C. When device junction temperature T_j further rises above overtemperature protection threshold, the device turns off all output drivers, pulls the $\overline{FLT}$ pin low with constant current sink to report fault, and sets the flag registers including FLAG_TSD and FLAG_ERR to 1.

The fault is latched in flag registers. When the junction temperature falls below $T_{TSD1} – T_{TSD1\_HYS}$, the device resumes all outputs and releases $\overline{FLT}$ pin pull-down. The master controller must write 1 to CLRFAULT to clears FLAG_TSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Overtemperature shutdown in NORMAL state

When the T_j rises too high above T_{TSD2}, 185 °C typically, NEX1324X-Q100 turns off the internal linear regulator, VLDO output to shut down all the analog and digital circuit.

The $\overline{FLT}$ pin is pulled down by constant current sink to report the fault, and the FLAG_POR and FLAG_ERR are all set to 1. When the T_j drops below $T_{TSD2} – T_{TSD2\_HYS}$, NEX1324X-Q100 restarts from POR state with all the registers cleared to default value and $\overline{FLT}$ pin released. The master controller must write 1 to CLR_POR to clear both FLAG_POR and FLAG_ERR after fault removal. The CLR_POR bit automatically returns to 0.

Communication loss diagnostic in NORMAL state

NEX1324X-Q100 monitors the UART interface for communication with an internal watchdog timer. Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer.

If the watchdog timer overflows, the device automatically switches to Fail-Safe state as indicated by external FM input.

- If FM = 0, the device switches to Fail-Safe state 0.
- If FM = 1, the device switches to Fail-Safe state 1.

The watchdog timer is programmable by 4-bit register WDTIMER. NEX1324X-Q100 can directly enter Fail-Safe states from normal mode by burning WDTIMER to 0xFh. Disabling the watchdog timer by setting WDTIMER to 0x0h prevents the device from getting into Fail-Safe state.

LED open-circuit diagnostics in NORMAL state

NEX1324X-Q100 integrates LED open-circuit diagnostics to allow users to monitor LED status in real time. The device monitors voltage difference between Vs and OUTXn to judge if there is any open-circuit failure. The V_{Vs} is also monitored in parallel with programmable threshold to determine if V_{Vs} is high enough for open-circuit diagnostics.

The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than t_{BLANK}. The t_{BLANK} is programmed by register BLANK.

If PWM on-time is less than t_{BLANK}, the device does not report any open-circuit fault.

- When the device supply voltage V_{Vs} is below the threshold $V_{LOWVSTH}$ set by register LOWVSTH, the LED open-circuit is not detected nor reported.
- When the voltage difference $V_{Vs} – V_{OUTXn}$ is below threshold $V_{OPEN\_th\_rise}$ with duration longer than t_{BLANK}, and the device supply voltage V_{Vs} is above the threshold $V_{LOWVSTH}$ set by register LOWVSTH, NEX1324X-Q100 pulls the $\overline{FLT}$ pin down with one pulsed current sink for 50 µs to report fault and set flag registers including FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR to 1.

In NORMAL state, the device does not take any actions in response to the LED open-circuit fault and waits for the master controller to determine the protection behavior. The fault is latched in flag registers. When the voltage difference $V_{Vs} – V_{OUTXn}$ rises above threshold $V_{OPEN\_th\_rise}$ with duration longer than t_{BLANK}, or the device's V_{Vs} is below the threshold $V_{LOWVSTH}$, the master controller must write 1 to CLRFAULT to clears FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

To minimize the limitations of the open threshold on system design, users can configure OPENTH bit to set the most suitable threshold, the setting as below:

- OPENTH=0 LED OPEN, rising threshold: V_{Vs} - V_{OUT} < 200 mV; falling threshold: V_{Vs} - V_{OUT} > 300 mV
- OPENTH=1 LED OPEN, rising threshold: V_{Vs} - V_{OUT} < 300 mV; falling threshold: V_{Vs} - V_{OUT} > 400 mV

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LED short-circuit diagnostics in NORMAL state

NEX1324X-Q100 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting OUTXn short to GND fault. The short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of t_{BLANK}. The t_{BLANK} is programmable by register BLANK.

If PWM on-time is less than t_{BLANK} the device cannot report any short-circuit fault. When the voltage V_{OUTXn} is below threshold $V_{SG\_th\_fall}$ with duration longer than deglitch timer length of t_{BLANK}, the device pulls the $\overline{FLT}$ pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SHORTCHXn, FLAG_OUT and FLAG_ERR.

In NORMAL state, the device does not take any actions in response to the LED short-circuit fault and waits for the master controller to determine the protection behavior. The fault is latched in flag registers. When the voltage V_{OUTXn} rises above threshold $V_{SG\_th\_rise}$ with duration longer than deglitch timer length of t_{BLANK}, the master controller must write 1 to CLRFAULT to clears FLAG_SHORTCHXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Single-LED short-circuit detection in NORMAL state (auto scan)

NEX1324X-Q100 integrates analog comparators to monitor all outputs with respect to two alternative threshold for single-LED short-circuit diagnosis. Setting the register SLSEN to 1 enables the single-LED short- circuit detection.

The single-LED, short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of $t_{BLANK} + t_{SLS\_deg}$. The t_{BLANK} is programmable by register BLANK. If PWM on-time is less than $t_{BLANK} + t_{SLS\_deg}$, the device cannot report any single-LED short-circuit fault. When the device supply voltage Vs is below the threshold $V_{LOWSUPTH}$ set by register LOWSUPTH, the single-LED short-circuit is not detected nor reported.

When the voltage V_{OUTXn} is below threshold V_{SLSTHx} with duration longer than deglitch timer length of $t_{BLANK} + t_{SLS\_deg}$, and the device supply voltage V_{SUPPLY} is above the threshold $V_{LOWSUPTH}$ set by register LOWSUPTH, the device pulls the ERR pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR.

NEX1324X-Q100 provides two alternative thresholds V_{SLSTH0} and V_{SLSTH1} for single-LED short-circuit detection selected by SLSTHOUTXn independently for each current output. The V_{SLSTH0} is selected for current OUTXn when SLSTHOUTXn is set to 0, however V_{SLSTH1} is selected when SLSLTHOUTXn is set to 1. The actual voltage value for V_{SLSTH0} and V_{SLSTH1} is programmable by two 7-bit registers SLSTH0 and SLSTH1 from 2.5 V to 18.375 V at 125 mV interval.

In NORMAL state, the device does not take any actions in response to the single-LED short-circuit fault and waits for the master controller to determine the protection behavior.

The fault is latched in flag registers. When the voltage V_{OUTXn} rises above threshold V_{SLSTHx} + 275 mV with duration longer than deglitch timer length of $t_{BLANK} + t_{SLS\_deg}$, or the device supply voltage V_{Vs} is below the threshold $V_{LOWSUPTH}$, the master controller must write 1 to register CLRFAULT to clears FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT automatically returns to 0.

MTP CRC error in NORMAL state

NEX1324X-Q100 implements MTP CRC check after loading the MTP code to configuration register in NORMAL state. The calculated CRC result is sent to register CALC_MTPCRC and compared to the data in register MTPCRC, which stores the CRC code for all MTP registers.

If the code in register CALC_MTPCRC is not matched to the code in register MTPCRC, NEX1324X-Q100 pulls the $\overline{FLT}$ pin down with pulsed current sink for 50 µs to report the fault and set the registers including FLAG_MTPCRC and FLAG_ERR to 1. NEX1324X-Q100 only loads MTP to corresponding registers one time during initialization state.

Reloading the MTP triggers the MTP CRC check. The master controller must write CLRFAULT to 1 to clear the fault flags, and the CLRFAULT bit automatically returns to 0. The CRC code algorithm for multiple bytes of binary data is based on the polynomial, $X^8 + X^5 + X^4 + 1$. The CRC code contains 8-bit binary code, and the initial value is FFh.

All bits code shift to MSB direction for 1 bit with three exclusive-OR calculation. A new CRC code for one byte input can be generated after repeating the 1-bit shift and three exclusive-OR calculation for eight times. Based on this logic, the CRC code can be calculated for all the MTP register byte.

When the MTP design for production is finalized, the corresponding CRC code based on the calculation must be burnt to MTP register MTPCRC together with other MTP registers at the end of production line. If the DC current for each output channel must be calibrated at the end of production for different LED brightness bin, the CRC code for each production

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devices must be calculated independent and burnt during the calibration. The CRC algorithm must be implemented into the LED calibration system at the end of production line.

Table 17. CRC calculation range

Register	Calculation range
CALC_MTPCRC	00h to 17h, 20h to 37h, 40h to 44h, 50h to 67h, 6Ah to 6Ch, 70h to 7Eh, 80h to 86h
CALC_CONFCRC	00h to 17h, 20h to 37h, 40h to 44h, 50h to 67h, 6Ah to 6Ch, 70h to 7Eh, 80h to 86h

Low V_{Vbat} warning detection in NORMAL state

When (AUTOSS=1) and LOWVBAT_FD= 1, NEX1324X-Q100 will compare ADC sample V_{Vbat} value with V_{Vbat} threshold, the threshold is set by register LOWVBATTH (the range is 4 V to 35 V, low V_{Vbat} threshold x 0.25 V + 4 V). When sampled V_{Vbat} < V_{Vbat} threshold, NEX1324X-Q100 will pull the FLT pin down with pulsed current sink for 50 µs to report fault and set flag registers including FLAG_LOWVBAT and FLAG_ERR. When LOWBAT_FD = 0, the device does not report this fault.

Communication loss diagnostic in NORMAL state

NEX1324X-Q100 monitors the UART interface for communication with an internal watchdog timer. Any successful non-broadcast communication with correct CRC and address matching target device automatically resets the timer.

If the watchdog timer overflows, device automatically switches to Fail-Safe state and sets the FLAG_FS to 1. The master controller can access NEX1324X-Q100 and writes 1 to CLR_FS to set the device to NORMAL state again when the communication recovers. The watchdog timer is programmable by 4-bit register WDTIMER. NEX1324X-Q100 can directly enter Fail-Safe state from NORMAL state by burning MTP of WDTIMER to Fh. Disabling the watchdog timer by setting WDTIMER to 0h prevents the device from getting into Fail-Safe state.

Fault masking

NEX1324X-Q100 provides fault masking capability using masking registers. The device is capable of masking faults by channels or by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG_OUT register, FLAG_ERR register, and ERR output.

Table 18 lists the detailed description for each fault mask register in NORMAL state. To disable diagnostics on a single channel, setting DIAGENOUTXn registers to 0 disables open-circuit, LED short-circuit and single-LED short circuit diagnostics of channel n and thus no fault of this channel is reported to FLAG_OPENOUTXn, FLAG_SHORTCHXn, FLAG_SLSOUTXn, FLAG_OUT or FLAG_ERR registers, or to the ERR pin output.

Fault mask function is the same under normal mode and Fail-Safe mode.

Table 18. Fault masking in NORMAL state

Fault detected	Mask register	FLAG name	$\overline{FLT}$ pin
V_{Vs} low warning	MASKLOWVS=1	FLAG_LOWVS=1	no action
	MASKLOWVS=0	FLAG_LOWVS=1 FLAG_ERR=1	one pulse pulled down for 50 µs
V_{Vs} undervoltage	MASKVSUV=1	FLAG_VSUV=1	no action
	MASKVSUV=0	FLAG_VSUV=1 FLAG_ERR=1	constant pulled down
Reference fault	MASKREF=1	FLAG_REF=1	no action
	MASKREF=0	FLAG_REF=1 FLAG_ERR=1	constant pulled down
Pre-thermal warning	MASKPRETSD=1	FLAG_PRETSD=1	no action
	MASKPRETSD=0	FLAG_PRETSD=1 FLAG_ERR=1	one pulse pulled down for 50 µs

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Fault detected	Mask register	FLAG name	$\overline{\text{FLT}}$ pin
Overtemperature protection	MASKTSD=1	FLAG_TSD=1	no action
	MASKTSD=0	FLAG_TSD=1 FLAG_ERR=1	constant pulled down
MTPCRC error	MASKMTPCRC=1	FLAG_MTPCRC=1	no action
	MASKMTPCRC=0	FLAG_MTPCRC=1 FLAG_ERR=1	one pulse pulled down for 50 µs
LED open-circuit fault	MASKOPEN=1	FLAG_OPENOUTn=1	no action
	MASKOPEN=0	FLAG_OPENOUTn=1 FLAG_OUT=1 FLAG_ERR=1	one pulse pulled down for 50 µs
LED short-circuit fault	MASKSHORT=1	FLAG_SHORTCHXn = 1	no action
	MASKSHORT=0	FLAG_SHORTCHXn=1 FLAG_OUT=1 FLAG_ERR=1	one pulse pulled down for 50 µs
Single-LED short-circuit fault	MASKSLS=1	FLAG_SLSOUTXn=1	no action
	MASKSLS=0	FLAG_SLSOUTXn=1 FLAG_OUT=1 FLAG_ERR=1	one pulse pulled down for 50 µs

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Table 19. Diagnostics table in NORMAL state

Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	$\overline{FLT}$ pin	Recovery
V_{Vbat} UVLO based on comparator	$V_{Vbat} < V_{POR\_fall}$	comparator	device switch to POR state	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR
VLDO UVLO based on comparator	$V_{VLDO} < V_{VLDO\_POR\_fall}$	comparator	device switch to POR state	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR
VLDO OV	$V_{VLDO} > V_{VLDO\_OV\_rise}$	comparator	no action	FLAG_LDOOV FLAG_ERR	constant pulled down	automatically recovers upon fault removal; clears fault flag with CLRFAULT
Low V_{Vbat} warning	$V_{Vbat} < V_{LOWVBATTH}$	ADC(AUTOSS=1) & LOWVBAT_FD=1	no action	FLAG_LOWVBAT (optional disable) FLAG_ERR(optional disable)	one pulse pulled down for 50 µs (optional disable)	clears fault flag with CLRFAULT
Low V_{Vs} warning	$V_{Vs} < V_{ADCLOWVSTH}$	ADC	disable fault type	FLAG_LOWVS FLAG_ERR (maskable)	one pulse pulled down for 50 µs (maskable)	clears fault flag with CLRFAULT
V_{Vs} undervoltage	$V_{Vs} < V_{Vs\_th\_fall}$	comparator or ADC(AUTOSS=1)	turn off all outputs	FLAG_VSUV FLAG_LOWVS FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flag with CLRFAULT
Reference fault	$V_{REF} < V_{REF\_SHORT\_th}$ or $I_{REF} < I_{REF\_OPEN\_th}$	comparator or ADC(AUTOSS=1)	no action	FLAG_REF FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Pre-thermal warning	$T_j > T_{PRETSD}$	comparator or ADC(AUTOSS=1)	no action	FLAG_PRETSD	one pulse pulled down for 50 µs (maskable)	clears fault flags with CLRFAULT
Overtemperature protection	$T_j > T_{TSD1}$	comparator	turn off all outputs	FLAG_PRETSD FLAG_TSD FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Overtemperature shutdown	$T_j > T_{TSD2}$	comparator	turn off VLDO	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR

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Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	$\overline{FLT}$ pin	Recovery
LED open-circuit fault (disable fault type)	$V_{Vs} - V_{OUTXn} < V_{OPEN\_th\_rise}$ $V_{Vs} > V_{LOWVSTH}$	PWM pulse width greater than $t_{(BLANK)}$ ENOUTXn=1 DIAGENOUTXn=1 comparator or ADC(AUTOSS=1)	no action	FLAG_OPENOUTn FLAG_OUT(maskable) FLAG_ERR (maskable)	one pulse pulled down for 50 µs (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Single-LED short circuit (disable fault type)	$V_{OUTXn} < V_{ADCSHORTTH}$ $V_{SUPPLY} > V_{ADCLOWVSTH}$	PWM pulse width greater than $T_{(BLANK)} + 3 \times T_{(CONV)}$ ENOUTXn=1 DIAGENOUTXn=1 ADC (AUTOSS=1)	no action	FLAG_ODDIAGCHn FLAG_OUT(maskable) FLAG_ERR (maskable)	one pulse pulled down for 50 µs (maskable)	clears fault flag with CLRFAULT
MTP-ROM CRC error	CALC_MTPCRC is different from MTPCRC	-	no action	FLAG_MTPCRC FLAG_ERR (maskable)	one pulse pulled down for 50 µs (maskable)	clears fault flag with CLRFAULT
Communication loss fault	$T_{WDTIMER}$ overflows	-	enters Fail-Safe states	FLAG_FS	no action	set CLRFS to 1 to set the device to NORMAL state
Unexpected V_{OUT} during channel disable	during channel disable time, $V_{OUTXn} > V_{SG\_th\_rise}$	OFFOUT_FD=1 ADC(AUTOSS=1)	no action	FLAG_OFFOUT (OFFOUT_FD=1) FLAG_ERR (OFFOUT_FD= 1)	one pulse pulled down for 50 µs (OFFOUT_FD = 1)	clears fault flag with CLRFAULT

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15.3.7. Diagnostic and protection in Fail-Safe state

In Fail-Safe state, NEX1324X-Q100 also detects failures and reports the status out by $\overline{FLT}$ pin or FLAG registers.

Table 21 lists the summary of the fault detection criteria and the device behavior after the fault is detected. Basically, NEX1324X-Q100 actively takes the action to turn off the failed output channels, retry on the failed channels, or restart the device to keep device operating without controlled by the master. The MTP register NV_OFAF can be used to set the fault behavior for LED open-circuit, LED short-circuit, and single-LED short-circuit faults.

The one-fails-all-fail behavior is selected when the register NV_OFAF is burnt to 1; otherwise, the one-fails-others-on behavior is chosen. NEX1324X-Q100 turns off all output channels when any type of LED fault is detected on any one of output channels for one-fails-all-fail behavior.

On the other hand, NEX1324X-Q100 only turns off the failed channel and keeps all other normal channels on. In Fail-Safe state, the fault flag registers of NEX1324X-Q100 still can be accessed again through UART interface in case the communication is rebuilt.

V_{Vbat} and V_{VLDO} undervoltage lockout diagnostics in Fail-Safe state

When V_{Vbat} or V_{VLDO} drops below its UVLO threshold, the device enters POR state. Upon voltage recovery, the device automatically switches to INIT state with FLAG_POR and FLAG_ERR set to 1. The master controller can write 1 to register CLRPOR to clear the FLAG_POR and FLAG_ERR, and the CLRPOR bit automatically returns to 0.

Low-supply warning diagnostics in Fail-Safe state

NEX1324X-Q100 continuously monitors the V_{Vs} and compares the results with internal threshold $V_{LOWVSTH}$ set by LOWVSTH for low supply voltage warning.

If the supply voltage is lower than threshold, the device sets flag registers including FLAG_LOWVS and FLAG_ERR to 1. The fault is latched in flag registers.

- When the supply voltage rises above low-supply warning threshold, the master controller must write register CLRFAULT to 1 to reset FLAG_LOWVS and FLAG_ERR. The CLRFAULT bit automatically returns to 0. The low-supply warning is also used to disable the LED open-circuit detection and single-LED short-circuit detection.
- When the voltage applied on Vs pin is higher than the threshold $V_{LOWVSTH}$, NEX1324X-Q100 enables LED open-circuit and single-LED short-circuit diagnosis.
- When V_{Vs} is lower than the threshold $V_{LOWVSTH}$, the device disables LED-open-circuit detection and single-LED short-circuit diagnosis.

Since when V_{Vs} drops below the maximum total LED forward voltage plus required V_{OUT_drop} at required current, NEX1324X-Q100 is not able to deliver sufficient current output to pull the voltage of each output channel as close as possible to the pin Vs. In this condition, the LED open-circuit fault or single-LED short circuit fault might be detected and reported by mistake. Setting the low-supply warning threshold high enough can prevent the LED open-circuit and single LED short-circuit fault being detected when V_{Vs} drops too low. The $V_{LOWVSTH}$ is programmable from 4 V to 35 V at 1 V interval.

V_{Vs} undervoltage diagnostics in Fail-Safe state

NEX1324X-Q100 provides internal analog comparator to monitor the supply voltage for undervoltage protection in Fail-Safe state. If the supply voltage falls below the internal threshold, $V_{Vs\_th\_fall}$, the device pulls the $\overline{FLT}$ pin low with constant current sink to report the fault and set flag registers including FLAG_VSUV and FLAG_ERR to 1.

The supply undervoltage detection is used to disable all current output.

- When V_{Vs} is lower than the threshold $V_{Vs\_th\_fall}$, the device disables every output to avoid the unwanted LED flickering or output fault triggered improperly.
- When the voltage applied on Vs pin rises above the threshold $V_{Vs\_th\_rise}$, NEX1324X-Q100 enables all current outputs automatically. The fault is latched in flag registers.
- When the supply voltage rises above $V_{Vs\_th\_rise}$, NEX1324X-Q100 releases $\overline{FLT}$ pin and the master controller must write register CLRFAULT to 1 to clears FLAG_VSUV and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

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Reference diagnostics in Fail-Safe state

NEX1324X-Q100 integrates diagnostics for REF resistor open and short fault in Fail-Safe state. The device monitors the reference current I_{REF} set by external resistor R_{REF}.

Use equation (6) to calculate the I_{REF}. If the current output from REF pin I_{REF} is lower than $I_{REF\_OPEN\_th}$, the reference resistor open-circuit fault is reported. The reference resistor short-circuit fault is reported if the voltage of REF pin V_{REF} is lower than $V_{REF\_SHORT\_th}$. The device pulls the $\overline{FLT}$ pin down with constant current sink and sets flag registers including FLAG_REF and FLAG_ERR to 1. The fault is latched in flag registers.

After the REF pin I_{REF} and $V_{REF\_SHORT\_th}$ recover to normal, the device releases $\overline{FLT}$ pin pull-down automatically and the master controller must send CLRFAULT to clear FLAG_REF and FLAG_ERR. The CLRFAULT automatically returns to 0. In Fail-Safe state, the device turns off all output channels when reference fault is detected. The device automatically recovers and turns on all enabled channels after fault removal.

Pre-thermal warning in Fail-Safe state

NEX1324X-Q100 has pre-thermal warning at typical 135 °C in Fail-Safe state.

- When the junction temperature T_j of NEX1324X-Q100 rises above pre-thermal warning threshold, the device reports pre-thermal warning and sets the flag registers including FLAG_PRETSD and FLAG_ERR to 1. The fault is latched in flag registers.
- When the junction temperature of NEX1324X-Q100 falls below pre-thermal warning threshold, the master controller must write 1 to CLRFAULT register to clear FLAG_PRETSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Overtemperature protection in Fail-Safe state

NEX1324X-Q100 has overtemperature protection at T_{TSD1}, typical 175 °C in Fail-Safe state. When the device junction temperature T_j further rises above overtemperature protection threshold, the device turns off all output drivers, pulls the $\overline{FLT}$ pin low with constant current sink to report fault, and sets the flag registers including FLAG_TSD and FLAG_ERR to 1. The fault is latched in flag registers.

When the junction temperature falls below $T_{TSD1} – T_{TSD1\_HYS}$, the device resumes all outputs and releases $\overline{FLT}$ pin pull-down. The master controller must write 1 to CLRFAULT to clear FLAG_TSD and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Overtemperature shutdown in Fail-Safe state

When the T_j rises too high above T_{TSD2}, typically 185 °C, NEX1324X-Q100 turns off the internal linear regulator, VLDO output to shut down all the analog and digital circuits. The $\overline{FLT}$ pin is pulled down by constant current sink to report the fault, and the FLAG_POR and FLAG_ERR are all set to 1.

When the T_j drops below $T_{TSD2} – T_{TSD2\_HYS}$, NEX1324X-Q100 restarts from POR state with all the registers clearsed to default value and $\overline{FLT}$ pin released. The master controller must write 1 to CLR_POR to clear both FLAG_POR and FLAG_ERR after fault removal. The CLR_POR bit automatically returns to 0.

LED open-circuit diagnostics in Fail-Safe state

NEX1324X-Q100 integrates LED open-circuit diagnostics to allow users to monitor LED status real time in Fail-Safe state. The device monitors voltage difference between Vs and OUTXn to judge if there is any open-circuit failure. The V_{Vs} is also monitored in parallel with programmable threshold to determine if supply voltage is high enough for open-circuit diagnostics. The open-circuit monitor is only effective during PWM-ON state with programmable minimal pulse width greater than t_{BLANK}.

The t_{BLANK} is programmed by register BLANK. If PWM on-time is less than t_{BLANK}, the device does not report any open-circuit fault. When the device supply voltage V_{Vs} is below the threshold $V_{LOWVSTH}$ set by register ADCLOWVSTH, the LED open-circuit fault is not detected nor reported.

When the voltage difference $V_{Vs} – V_{OUTXn}$ is below threshold $V_{OPEN\_th\_rise}$ with duration longer than t_{BLANK}, and the device supply voltage V_{Vs} is above the threshold $V_{LOWVSTH}$, NEX1324X-Q100 pulls the $\overline{FLT}$ pin down with constant current sink to report fault and set flag registers including FLAG_OPENOUTXn, FLAG_OUT and FLAG_ERR to 1.

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In Fail-Safe state, NEX1324X-Q100 shuts down the normal current regulation and PWM duty cycle for the error output, then the device sources a current I_{retry} to faulty output every t_{retry}, typically 10 ms for retrying. I_{retry} is programed by ODIOUT register. The current I_{retry} can be calculated with the equation (7).

When the voltage difference $V_{Vs} – V_{OUTXn}$ of error output rises above threshold $V_{OPEN\_th\_rise}$ with duration longer than t_{BLANK}, or the supply voltage V_{Vs} is above the threshold $V_{LOWVSTH}$, the device automatically resumes the normal current and PWM duty cycle setup and releases the $\overline{FLT}$ pin.

$$I_{retry} = \frac{CONF_{ODIOUT} \times 4 + 4}{64} \times I_{full\_range} \quad (7)$$

I_{retry} is programmable from 0 to 15.

Use equation (7) to calculate I_{full_range}.

The fault is latched in flag registers. When the open-circuit failure is removed, the master controller must write 1 to CLRFAULT to clear FLAG_OPENCHn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

To meet the non-retry requirement for some application, NEX1324X-Q100 adds one CONF register option to close retry function as below, this function is applicable to all retry scenarios.

- DISRETRY: Fail-Safe mode retry function enable bit
- DISRETRY=0: under Fail-Safe mode, when LED OPEN or LED SHORT appears, NEX1324X-Q100 will auto retry to open the channel.
- DISRETRY=1: under Fail-Safe mode, when LED OPEN or LED SHORT appears, NEX1324X-Q100 will keep the channel off, and latch the status, unless the communication recovery and the fault flag is clearsed.

LED short-circuit diagnostics in Fail-Safe state

NEX1324X-Q100 has internal analog comparators to monitor all channel outputs with respect to a fixed threshold for reporting OUTXn short to GND fault in Fail-Safe state. The short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of t_{BLANK}. The t_{BLANK} is programmable by register BLANK. If PWM on-time is less than t_{BLANK}, the device cannot report any short-circuit fault.

When the voltage V_{OUTXn} is below threshold $V_{SG\_th\_fall}$ with duration longer than deglitch timer length of t_{BLANK}, the device pulls $\overline{FLT}$ pin down with constant current sink to report fault and set flag registers including FLAG_SHORTCHn, FLAG_OUT and FLAG_ERR.

In Fail-Safe state, NEX1324X-Q100 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current to faulty output every t_{retry}, 10 ms for retrying. I_{retry} is programed by ODIOUT register. Use equation (7) to calculate the current I_{retry}.

When the voltage V_{OUTXn} of error output rises above threshold $V_{SG\_th\_rise}$ with duration longer than t_{BLANK}, the device automatically resumes the normal current and PWM duty cycle setup and releases the $\overline{FLT}$ pin. The fault is latched in flag registers. When the short-circuit failure is removed, the master controller must write 1 to CLRFAULT to clear FLAG_SHORTOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT bit automatically returns to 0.

Single-LED short-circuit detection in Fail-Safe state

NEX1324X-Q100 integrates analog comparators to monitor all outputs with respect to two alternative threshold for single-LED short-circuit diagnostic in Fail-Safe state. Setting the register SLSEN to 1 enables the single-LED short-circuit detection.

The single-LED short-circuit detection is only effective during PWM-ON state with programmable minimal pulse width of t_{BLANK}. The t_{BLANK} is programmable by register BLANK.

If PWM on-time is less than t_{BLANK}, the device cannot report any single-LED short-circuit fault.

When the device supply voltage V_{Vs} is below the threshold $V_{LOWVSTH}$ set by register ADCLOWVSTH, the single-LED short-circuit is not detected nor reported.

When the voltage V_{OUTXn} is below threshold $V_{SLSTHOUTXn}$ with duration longer than deglitch timer length of t_{BLANK}, and the device supply voltage V_{Vs} is above the threshold $V_{LOWVSTH}$, the device pulls the $\overline{FLT}$ pin down with constant current sink to report fault and set flag registers including FLAG_SLSTHOUTXn, FLAG_OUT and FLAG_ERR.

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NEX1324X-Q100 provides two alternative threshold $V_{ADCSHORTTH0}$ and $V_{ADCSHORTTH1}$ for single-LED short-circuit detection selected by SLSTHOUTXn independently for each current output. The $V_{ADCSHORTTH0}$ is selected for current OUTXn when SLSTHOUTXn is set to 0, however $V_{ADCSHORTTH1}$ is selected when SLSTHOUTXn is set to 1.

The actual voltage value for V_{SLSTH0} and V_{SLSTH1} is programmable by two 7-bit registers SLSTH0 and SLSTH1 from 2.5 V to 15.875 V at 125 mV interval. In Fail-Safe state, NEX1324X-Q100 shuts down the normal current regulation and PWM duty cycle for the faulty output, then the device sources a pulse current, I_{OUTXn} programed by IOUTXn register to the faulty output every t_{SLS_Retry}, 10 ms for retrying.

When the voltage V_{OUTXn} of error output rises above threshold V_{SLSTHx} + 275 mV with duration longer than $t_{BLANK)}$ + t_{SLS_deg} during retrying, or the supply voltage V_{Vs} is below the threshold $V_{LOWSUPTH}$, the device automatically resumes the normal current and PWM dutycycle setup and releases the $\overline{FLT}$ pin.

The fault is latched in flag registers. When the single-LED short-circuit fault is removed, the master controller must write 1 to register CLRFAULT to clear FLAG_SLSOUTXn, FLAG_OUT and FLAG_ERR. The CLRFAULT automatically returns to 0.

MTP CRC error in Fail-Safe state

NEX1324X-Q100 automatically reloads all MTP code into the corresponding configuration registers every time after entering the Fail-Safe state. NEX1324X-Q100 implements a MTPCRC check after loading the MTP code to configuration register in Fail-Safe state.

The calculated CRC results are sent to register CALC_MTPCRC and compared to the data in MTP register NV_CRC, which stores the CRC code for all MTP registers. If the code in register CALC_MTPCRC is not matched with the code in register NV_CRC, NEX1324X-Q100 turns off all channels output, pulls the $\overline{FLT}$ pin down with constant current sink to report the fault, and sets the registers including FLAG_MTPCRC and FLAG_ERR to 1. The CRC code for all the MTP registers must be burnt into MTP register MTPCRC at the end of production line. The CRC code algorithm is described in MTP CRC Error in NORMAL state.

Fault masking in Fail-Safe state

To disable diagnostics on a single channel in Fail-Safe state, burning MTP of DIAGENOUTXn registers to 0 disables open-circuit, LED short-circuit and single-LED short-circuit diagnostics of channel x, and thus no fault of this channel is reported to FLAG_OPENOUTXn, FLAG_SHORTCHXn, FLAG_SLSOUTXn, FLAG_OUT or FLAG_ERR registers, or to the ERR output.

Table 20. Fault masking register in NORMAL state

Fault detected	Mask register	FLAG name	$\overline{FLT}$ pin
Low-supply warning	MASKLOWVS = 1	FLAG_LOWVS = 1	no action
	MASKLOWVS = 0	FLAG_LOWVS = 1 FLAG_ERR = 1	no action
Supply undervoltage	MASKSUPUV = 1	FLAG_SUPUV = 1	no action
	MASKSUPUV = 0	FLAG_SUPUV = 1 FLAG_ERR = 1	constant pulled down
Reference fault	MASKREF = 1	FLAG_REF = 1	no action
	MASKREF = 0	FLAG_REF = 1 FLAG_ERR = 1	constant pulled down
Pre-thermal warning	MASKPRETSD = 1	FLAG_PRETSD = 1	no action
	MASKPRETSD = 0	FLAG_PRETSD = 1 FLAG_ERR = 1	no action
Overtemperature protection	MASKTSD = 1	FLAG_TSD = 1	no action
	MASKTSD = 0	FLAG_TSD = 1 FLAG_ERR = 1	constant pulled down
MTPCRC error	MASKMTPCRC = 1	FLAG_MTPCRC = 1	no action
	MASKMTPCRC = 0	FLAG_MTPCRC = 1 FLAG_ERR = 1	constant pulled down

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Fault detected	Mask register	FLAG name	$\overline{\text{FLT}}$ pin
LED open-circuit fault	MASKOPEN = 1	FLAG_OPENOUTXn = 1	no action
	MASKOPEN = 0	FLAG_OPENOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	constant pulled down
LED short-circuit fault	MASKSHORT= 1	FLAG_SHORTOUTXn= 1	no action
	MASKSHORT= 0	FLAG_SHORTOUTXn= 1 FLAG_OUT = 1 FLAG_ERR = 1	constant pulled down
Single-LED short-circuit fault	MASKSLS = 1	FLAG_SLSOUTXn = 1	no action
	MASKSLS = 0	FLAG_SLSOUTXn = 1 FLAG_OUT = 1 FLAG_ERR = 1	Constant pulled down

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Table 21. Diagnostics table in Fail-Safe state

Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	$\overline{FLT}$ pin	Recovery
V_{Vbat} UVLO Based on comparator	$V_{Vbat} < V_{POR\_fall}$	comparator	device switch to POR state	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR
VLDO UVLO Based on comparator	$V_{VLDO} < V_{VLDO\_POR\_fall}$	comparator	device switch to POR state	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR
Low-supply warning	$V_{Vs} < V_{LOWVSTH}$	ADC	disable fault type	FLAG_LOWVS FLAG_ERR (maskable)	no action	clears fault flag with CLRFAULT
V_{Vs} undervoltage	$V_{Vs} < V_{Vs\_th\_fall}$	comparator	turn off all outputs	FLAG_VSUV FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flag with CLRFAULT
Reference fault	$V_{REF} < V_{REF\_SHORT\_th}$ or $I_{REF} < I_{REF\_OPEN\_th}$	comparator	turn off all outputs	FLAG_REF FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Pre-thermal warning	$T_j > T_{PRETSD}$	comparator	no action	FLAG_PRETSD FLAG_ERR(maskable)	no action	clears fault flags with CLRFAULT
Overtemperature protection	$T_j > T_{TSD1}$	comparator	turn off all outputs	FLAG_TSD FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Overtemperature shutdown	$T_j > T_{TSD2}$	comparator	turn off VLDO	FLAG_POR FLAG_ERR	constant pulled down	device switch to INIT state when all voltage rails are good; clears fault flag with CLR_POR
LED open-circuit fault (disable fault type)	$V_{Vs} - V_{OUTXn} < V_{OPEN\_th\_rise}$ $V_{Vs} > V_{LOWVSTH}$	PWM pulse width greater than $t_{(BLANK)}$ ENOUTXn=1 DIAGENOUTXn=1	turn off the failed outputs and retry every 10 ms	FLAG_OPENOUTn FLAG_OUT(maskable) FLAG_ERR (maskable)	constant pulled down (maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
Single-LED short circuit (disable fault type)	$V_{OUTXn} < V_{ADCSHORTTH}$ $V_{SUPPLY} > V_{ADCLOWVSTH}$	PWM pulse width greater than $T_{(BLANK)} + 3 \times T_{(CONV)}$ ENOUTXn=1 DIAGENOUTXn=1 SLSEN=1	no action	FLAG_SLSOUTXn FLAG_OUT(maskable) FLAG_ERR (maskable)	constant pulled down(maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flag with CLRFAULT

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Fault type	Detection criteria	Conditions and method	Fault actions	Fault output	$\overline{FLT}$ pin	Recovery
LED short-circuit fault	$V_{OUTXn} < V_{SG\_th\_rise}$	PWM pulse width greater than $t_{(BLANK)}$ ENOUTXn=1 DIAGENOUTXn=1	turn off the failed outputs and retry every 10 ms	FLAG_SHORTOUTXn FLAG_OUT(maskable) FLAG_ERR (maskable)	constant pulled down(maskable)	automatically recovers and releases $\overline{FLT}$ pin upon fault removal; clears fault flags with CLRFAULT
MTP CRC error	CALC_MTPCRC is different MTPCRC		turn off all outputs	FLAG_MTPCRC FLAG_ERR (maskable)	constant pulled down (maskable)	clears fault flags with CLRFAULT

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15.3.8. OFAF setup in Fail-Safe state

NEX1324X-Q100 has a unique setup for failure behaviors in Fail-Safe state. If there is a failure detected in Fail-Safe state, NEX1324X-Q100 automatically reacts to the failure. The register OFAF determines whether the result behavior of output failure is one-fails-all-fail or one-fails-others-on.

In Fail-Safe state, NEX1324X-Q100 shuts down all enabled current outputs except the faulty output when OFAF is set to 1. Otherwise, NEX1324X-Q100 keeps regulation for all enable current outputs except the faulty output when OFAF is set to 0. Refer to Table 22 for more details.

15.3.9. $\overline{FLT}$ output

The $\overline{FLT}$ pin is a programmable fault indicator pin. This pin can be used as an interrupted output to master controller in case there is any fault in NORMAL state. In Fail-Safe states, the $\overline{FLT}$ pin can be used as an output to other $\overline{FLT}$ pin of other NEX1324X-Q100 to achieve one-fails-all-fail at system level. The $\overline{FLT}$ pin is an open-drain output with current limit up to $I_{PD(ERR)}$. Nexperia recommends a < 10 kΩ external pull-up resistor from the $\overline{FLT}$ pin to the same IO voltage of the master controller.

In NORMAL state, when a fault is triggered, depending on the fault type, the $\overline{FLT}$ pin is either pulled down constantly or pulled down for a single pulse. After an $\overline{FLT}$ output is triggered, the master controller must take action to deal with the failure and reset the fault flag. For non-critical faults, NEX1324X-Q100 pulls down the $\overline{FLT}$ pin with a duration of 50 µs and release; for critical faults, device constantly pulls down $\overline{FLT}$ as described in Table 19. In NORMAL state, basically, NEX1324X-Q100 only reports the faults to the master controller for most of the failure and takes no actions except supply or LDO UVLO, reference fault, and overtemperature. The master controller determines what action to take according to the type of failure.

NEX1324X-Q100 provides a forced-error feature to validate the error feedback-loop integrity in NORMAL state. In NORMAL state, if the microcontroller sets FORCEERR to 1, the FLAG_ERR is set 1 and pulls down $\overline{FLT}$ output with a pulse of 50 µs accordingly. The FORCEERR automatically returns to 0.

In Fail-Safe states, the $\overline{FLT}$ pin is used as fault bus. When there is any output failure reported, the $\overline{FLT}$ is pulled down by internal current sink $I_{PD(ERR)}$. NEX1324X-Q100 monitors the voltage of the $\overline{FLT}$ pin. If the one-fails-all-fail diagnostics is enabled by setting register OFAF to 1, all current output channels are turned off, as well as diagnostics, when the $\overline{FLT}$ pin voltage is low. If register OFAF is 0, the device only turns off the failed channel with alive channels diagnostics enabled.

Table 22. One-Fails-All-Fail feature in Fail-Safe state

$\overline{FLT}$ pin	**OFAF = 1**	**OFAF = 0**
$\overline{FLT}$ pulled low internally	all OUT channels OFF except failure detected OUT retries every 10 ms	only failure detected OUT OFF
$\overline{FLT}$ pulled low externally	all OUT channels OFF	all OUT channels ON

If multiple NEX1324X-Q100 devices are used in one application, tying the $\overline{FLT}$ pins together achieves the one-fails-all-fail behavior in Fail-Safe states without master controlling. Any one of NEX1324X-Q100 reports fault by pulling the $\overline{FLT}$ pin to low, and the low voltage on ERR bus is detected by other NEX1324X-Q100 as Fig. 41 illustrates. If the register OFAF is set to 1 for all NEX1324X-Q100 devices having the $\overline{FLT}$ pins tied together, all NEX1324X-Q100 devices turn off current for all output channels.

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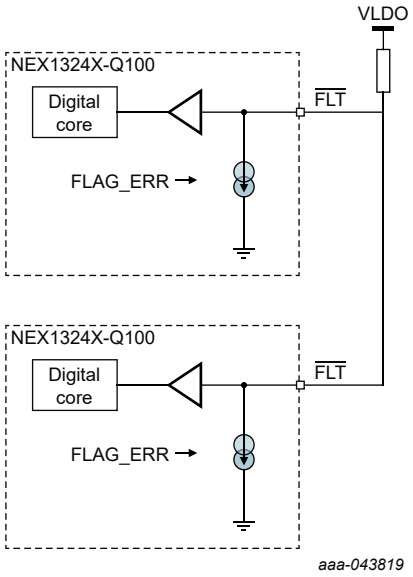

Fig. 41. Fault pin internal diagram

15.4. Device functional modes

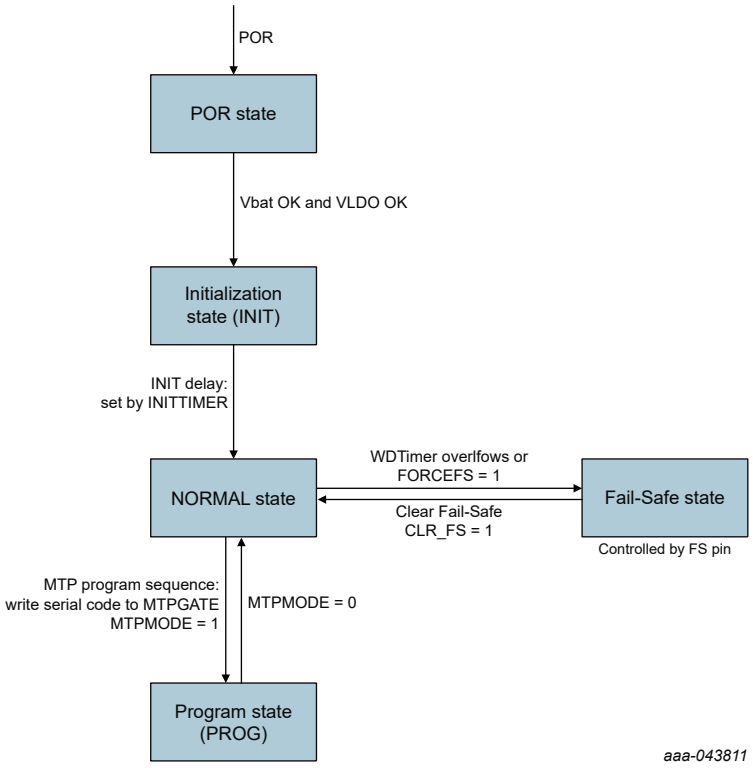

Fig. 42. Device functional mode state machine

15.4.1. POR state

Upon powering up, NEX1324X-Q100 enters POWER_ON_RESET (POR) state. In this state, registers are cleared to default value, outputs are disabled, and the device cannot be accessed through the differential data interface (UART). After both Vbat input and the VLDO output are above their UVLO threshold, the device switches to INITIALIZATION state (INIT). If any of the supply fails below UVLO threshold in other states, the device immediately switches to POR state.

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15.4.2. INITIALIZATION state

The INITIALIZATION state is designed to allow master controller to have enough time to power up before the device automatically gets into Fail-Safe states. INIT mode has a configurable delay programmed by 4-bit register NV_INITTIMER. After the delay counter is reached, the device changes to NORMAL state.

In INIT state, the communication between master controller and NEX1324X-Q100 is enabled through the differential data interface (UART). In INITIALIZATION state, the device automatically loads register map default values, which can be programmed in corresponding MTP. The master controller sets CLRPOR to 1 in INITIALIZATION state, the device immediately switches to NORMAL state. Only write CLR_POR to NEX1324X-Q100 in INITIALIZATION state.

15.4.3. NORMAL state

After NEX1324X-Q100 is in NORMAL state, the device operates under master control for LED animation and diagnostics using UART interface. NEX1324X-Q100 integrates a watchdog timer to monitor the communication on the differential data interface (UART). The watchdog timer is programmable by a 4-bit register WDTIMER for 13 options. The timer in NEX1324X-Q100 starts to count when there is no instruction received from the master controller.

NEX1324X-Q100 enters Fail-Safe states when the timer overflows. The device can be also forced into Fail-Safe states anytime in NORMAL state by setting FORCEFS to 1. The FORCEFS register automatically returns to 0.

15.4.4. Fail-Safe state

When NEX1324X-Q100 is entering Fail-Safe state from NORMAL state, all the registers are set to default value or reloaded from MTP. The differential data interface (UART) keeps alive in Fail-Safe state. Setting FORCEFS to 1 forces the device into Fail-Safe state from NORMAL state. NEX1324X-Q100 can quit from Fail-Safe state to NORMAL state by setting CLR_FS to 1 with FLAG_FS register cleared.

15.4.5. PROGRAM state

NEX1324X-Q100 can enter MTP PROGRAM state by writing multiple configuration registers to MTPGATE and setting 1 to MTPMODE. For details of getting into PROGRAM state, refer to Section 15.4.5.2.

15.4.5.1. UART over CAN protocol

NEX13240-Q100 integrates UART compliant controller, while NEX13241-Q100 integrates a CAN transceiver, the structure is showed in Fig. 43. NEX13240-Q100 is compliant with the UART, the data format is similar to UART. The signal input to NEX13241-Q100 is at the differential CAN physical electrical level, and the protocol is UART-based.

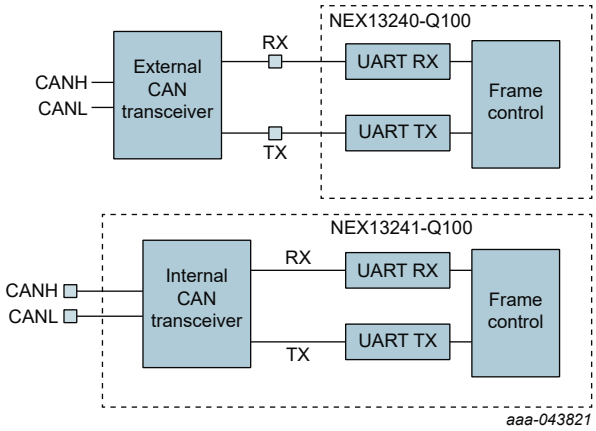

Fig. 43. Interface structure

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Differential data interface (UART) address setting

NEX1324X-Q100 supports a maximum of 27 slave devices. NEX1324X-Q100 has three pin-outs including ADDR2, ADDR1, and ADDR0 for slave address configuration. Different configurations allow each pin to support three statuses as shown in Table 23.

If EXTADDR = 0, the device uses DEVADDR [3] code together with external inputs on ADDR2, ADDR1 and ADDR0 as shown in Table 24, and ignores M status.

If EXTADDR = 1, the device uses external inputs on ADDR2, ADDR1 and ADDR0 to set 27 slaves as shown in Table 25. In this mode, ADDR2, ADDR1 and ADDR0 can support M status.

Table 23. Address pin status assessment

Status	Settings
0	tie directly (0 Ω) to GND
M	tie 30 kΩ to GND
1	option 1: tie 90 kΩ to GND option 2: tie directly to VCC

Table 24. Address setting: EXTADDR = 0

Address setting (EXTADDR = 0)				
Address (Decimal)	Bit 3	Bit 2	Bit 1	Bit 0
	NV_DEVADDR [3]	ADDR2	ADDR1	ADDR0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Table 25. Address setting: EXTADDR = 1

	Address setting (EXTADDR = 1)			
Slave address	Address (Decimal)	ADDR2	ADDR1	ADDR0
0	0	0	0	0
1	1	0	0	1
2	2	0	1	0
3	3	0	1	1
4	4	1	0	0
5	5	1	0	1
6	6	1	1	0
7	7	1	1	1

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	Address setting (EXTADDR = 1)			
Slave address	Address (Decimal)	ADDR2	ADDR1	ADDR0
8	8	0	0	M
9	9	0	1	M
10	10	1	0	M
11	11	1	1	M
12	12	0	M	0
13	13	0	M	1
14	14	1	M	0
15	15	1	M	1
16	16	M	0	0
17	17	M	0	1
18	18	M	1	0
19	19	M	1	1
20	20	0	M	M
21	21	1	M	M
22	22	M	0	M
23	23	M	1	M
24	24	M	M	0
25	25	M	M	1
26	26	M	M	M

Status response

When NEX1324X-Q100 works as a slave device receiving a non-broadcast frame, it first verifies the CRC byte. After CRC check is succeeded, NEX1324X-Q100 sends out the device status of FLAG_ERR register byte followed by CRC byte. The response is disabled by setting register ACKEN to 0. The response sent from NEX1324X-Q100 is enabled by default.

Every communication requires CRC verification to ensure the integrity of the data transaction. In broadcast mode, NEX1324X-Q100 does not send out a response.

Synchronization byte

The first byte data sent from the master controller to NEX1324X-Q100 is synchronization frame (SYNC). The master controller sends the clock signal to V through outputting 01010101 binary code in first frame.

NEX1324X-Q100 adaptively uses the same clock to communicate with master by synchronization of internal high frequency clock. To prevent clock drift over time, the synchronization byte is always required for each new message.

Device address byte

The device address byte, DEV_ADDR frame follows the SYNC frame. There is total 8-bit binary code in the device address byte. Table 26 provides detailed definition for each bit function. The DEVICE_ADDR register is required to set to 0000b for broadcast mode, otherwise the broadcast mode cannot be enabled. The broadcast mode is only effective for the writing mode. The READ/WRITE bit must be 1 for the broadcast mode.

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Table 26. DEV_ADDR byte

Bit	Field	Description
3-0	DEVICE_ADDR	target device address
5-4	DATA_LENGTH	00b: single-byte mode with 1 byte of data 01b: bust mode with 4 bytes of data 10b: burst mode with 16 bytes of data 11b: burst mode with 24 bytes of data
6	BROADCAST	broadcast mode 1: broadcast (DEVICE_ADDR =0000b) 0: single-device only
7	READ/WRITE	read/write mode 1: write mode 0: read mode

To support more than 16 slaves, we will use the broadcast bit as address bit when the amount of slave address is higher than 15, the details of DEV_ADDR byte for different slaves are listed in Table 27.

Table 27. Device address byte

DEV_ADDR byte				
Read/Write[7]	Broadcast[6]	Data length[5:4]	Device_ADDR[3:0]	Read/Write slave
Write: 1 Read: 0	0	00: 1 byte 01: 4 bytes 10: 16 bytes 11: 24 bytes	0	slave 0
	0		1	slave 1
	0		2	slave 2
	0		3	slave 3
	0		4	slave 4
	0		5	slave 5
	0		6	slave 6
	0		7	slave 7
	0		8	slave 8
	0		9	slave 9
	0		A	slave 10
	0		B	slave 11
	0		C	slave 12
	0		D	slave 13
	0		E	slave 14
	0		F	slave 15
	1		0	broadcast mode
	1		1	slave 16
	1		2	slave 17
	1		3	slave 18
	1		4	slave 19
	1		5	slave 20
	1		6	slave 21
	1		7	slave 22
	1		8	slave 23

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DEV_ADDR byte				
	1		9	slave 24
	1		A	slave 25
	1		B	slave 26

Registers lock

NEX1324X-Q100 provides registers content lock feature to prevent unintended modification of registers. There are four register lock bits for different types of registers covering all registers as Table 28 specifies. Nexperia recommends locking the register after the register writes operations.

Table 28. Registers lock table

Register IP name	Address	Lock register name	Lock register default
BRT (PWMMx)	00h to 17h	BRTLOCK	0 (unlock)
BRT (PWMLx)	20h to 37h		
BRT	40h to 44h		
IOUT	50h to 67h	IOUTLOCK	1 (lock)
CONF_FD	6Ah to 6Ch	CONFLOCK	1 (lock)
CONF	70h to 83h	CONFLOCK	1 (lock)
CONF	84h to 87h	always locked except in EEPROM program state	
CTRL (ADCCH and CLR)	90h and 91h	no lock register	-
CTRL	92h to 95h	unlock by sending serial code to CTRLGATE register	
CTRL (CTRLGATE)	96h	no lock register	-
CTRL (EEP)	97h	unlock by sending serial code to EEPGATE register	
CTRL (EEPGATE)	98h	no lock register	-

Below instructions are required to access and exit the CTRL (92h to 95h) register.

- Write 43h, 4Fh, 44h, 45h to 8-bit register CTRLGATE one-byte by one-byte sequentially to access.
- Write any 8-bit data to register CTRLGATE to exit active mode of the CTRL register.
- Write any data to register CTRLGATE also reset LOCK register (93h) to default value.

Register default data

NEX1324X-Q100 has three types of registers. The register IP name BRT with address between 00h to 17h, 20h to 37h and 40h to 44h, have the same set of MTP. These registers reset to 00h from POR or setting 1 to REGDEFAULT, and they load the code from the corresponding MTP value by the following operations:

- NEX1324X-Q100 enters Fail-Safe state by watchdog timer overflow.
- Writing FORCEFS to 1 to force NEX1324X-Q100 into Fail-Safe state.
- Writing MTPLOAD to 1 to load all corresponding MTP content.
- Writing MTPMODE to 1 to enter MTP program state.

The register IP name IOUT and CONF with address between 50h to approximately 67h and 70h to approximately 87h, have the same set of MTP. These registers always load MTP value through following operations:

- NEX1324X-Q100 starts from POR.
- NEX1324X-Q100 restarts from Vbat or LDO UVLO triggered.
- NEX1324X-Q100 enters Fail-Safe state by watchdog timer overflow.
- Writing FORCEFS to 1 to force NEX1324X-Q100 into Fail-Safe state.
- Writing MTPLOAD to 1 to load all corresponding MTP content.
- Writing REGDEFAULT to 1 to reset all registers to default code.

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- Writing MTPMODE to 1 to enter MTP program state.

The register IP name CTRL and FLAG with address between 90h to 98h and A0h to approximately AFh have no corresponding MTP cells. These registers always set to manufacture default value by following operation:

- NEX1324X-Q100 starts from POR.
- NEX1324X-Q100 restarts from Vbat or LDO UVLO triggered.

Table 29. Registers default value table

Register IP name	Register address	POR default and soft reset	REG Default	EEPLOAD	Fail-Safe state	EEPMODE
BRT (PWMMx)	00h to 17h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
BRT (PWMLx)	20h to 37h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
BRT	40h to 44h	00h	00h	Load EEPROM	Load EEPROM	Load EEPROM
IOUT	50 to 67h	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM
CONF_FD	6Ah to 6Ch	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM
CONF	70h to 87h	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM	Load EEPROM
CTRL	90h to 98h	default	no action	no action	only reset 93h to 03h, no action on other registers	set 93h to 00h
FLAG	A0 to AFh	default / Manufacture	only clear FLAG_POR to 00h no action on other registers	no action	no action	no action
FLAG_FD	B1h to B3h	default / manufacture	only clear FLAG_POR to 00h no action on other registers	no action	no action	no action

15.4.5.2. MTP Programming

NEX1324X-Q100 has a user-programmable MTP with high reliability for automotive applications. All the MTP registers can be burnt through writing the target data into its corresponding register. NEX1324X-Q100 supports two solutions for individual chip selection through pulling the REF pin high or through device address configuration by address pin.

Chip selection by pulling REF pin high

NEX1324X-Q100 supports using REF pin as chip-select during MTP programming. Considering multiple NEX1324X-Q100 devices connected on one UART bus before burning MTP, the slave address for all NEX1324X-Q100 is all same before programming in case internal MTP register DEVADDR is used for slave address setup.

The MTP burning instruction can be sent to target NEX1324X-Q100 by pulling the REF pin of the target NEX1324X-Q100 to 5 V. After the REF pin is pulled up to 5 V, NEX1324X-Q100 ignores the device address setup by ADDR2/ADDR1/ADDR0 pins or MTP programmed device address in DEVADDR.

The master controller must send out data to target NEX1324X-Q100 with device address as 0h and not in broadcast mode.

Chip selection by ADDR pins configuration

NEX1324X-Q100 also supports using configuration on ADDR2/ADDR1/ADDR0 pins to determine the slave address for NEX1324X-Q100 if multiple NEX1324X-Q100 devices are connected on the same differential data bus.

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Nexperia recommends using this approach for applications of multiple NEX1324X-Q100 in the same differential data bus. The master controller can send out register data to target NEX1324X-Q100 with device address matched to the ADDR2/ ADDR1/ADDR0 pins configuration and not in broadcast mode.

MTP register access and burn

After selecting the target NEX1324X-Q100 for MTP burning, the master controller must send a serial of data bytes to register MTPGATE, set 1 to MTPMODE one by one in below sequence to finally enable the MTP register access. Each data written must be a single-byte operation instead of burst-mode operation. For detailed program sequence, refer to NEX1324X-Q100 configuration guide and Section 15.5.

MTP program state exit

The REF pin can be released after MTP burning if it is pulled high to 5 V for chip selection. The REF pin must be kept high during all MTP program state. NEX1324X-Q100 can quit the MTP program state to normal state after burning by writing 0 to register MTPMODE. Nexperia recommends reloading the MTP data to the registers after MTP burning by setting 1 to REGDEFAULT.

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15.5. Register map

Table 30. Register map

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default	EEPROM default
00h	PWMMA0	PWMOUTA0								00h	FFh
01h	PWMMA1	PWMOUTA1								00h	FFh
02h	PWMMA2	PWMOUTA2								00h	FFh
03h	PWMMB0	PWMOUTB0								00h	FFh
04h	PWMMB1	PWMOUTB1								00h	FFh
05h	PWMMB2	PWMOUTB2								00h	FFh
06h	PWMMC0	PWMOUTC0								00h	FFh
07h	PWMMC1	PWMOUTC1								00h	FFh
08h	PWMMC2	PWMOUTC2								00h	FFh
09h	PWMMD0	PWMOUTD0								00h	FFh
0Ah	PWMMD1	PWMOUTD1								00h	FFh
0Bh	PWMMD2	PWMOUTD2								00h	FFh
0Ch	PWMME0	PWMOUTE0								00h	FFh
0Dh	PWMME1	PWMOUTE1								00h	FFh
0Eh	PWMME2	PWMOUTE2								00h	FFh
0Fh	PWMMF0	PWMOUTF0								00h	FFh
10h	PWMMF1	PWMOUTF1								00h	FFh
11h	PWMMF2	PWMOUTF2								00h	FFh
12h	PWMMG0	PWMOUTG0								00h	FFh
13h	PWMMG1	PWMOUTG1								00h	FFh
14h	PWMMG2	PWMOUTG2								00h	FFh
15h	PWMMH0	PWMOUTH0								00h	FFh
16h	PWMMH1	PWMOUTH1								00h	FFh
17h	PWMMH2	PWMOUTH2								00h	FFh

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ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default	EEPROM default
20h	PWMLA0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTA0				00h	0Fh
21h	PWMLA1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTA1				00h	0Fh
22h	PWMLA2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTA2				00h	0Fh
23h	PWMLB0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTB0				00h	0Fh
24h	PWMLB1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTB1				00h	0Fh
25h	PWMLB2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTB2				00h	0Fh
26h	PWMLC0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTC0				00h	0Fh
27h	PWMLC1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTC1				00h	0Fh
28h	PWMLC2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTC2				00h	0Fh
29h	PWMLD0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTD0				00h	0Fh
2Ah	PWMLD1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTD1				00h	0Fh
2Bh	PWMLD2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTD2				00h	0Fh
2Ch	PWMLE0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTE0				00h	0Fh
2Dh	PWMLE1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTE1				00h	0Fh
2Eh	PWMLE2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTE2				00h	0Fh
2Fh	PWMLF0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTF0				00h	0Fh
30h	PWMLF1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTF1				00h	0Fh
31h	PWMLF2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTF2				00h	0Fh
32h	PWMLG0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTG0				00h	0Fh
33h	PWMLG1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTG1				00h	0Fh
34h	PWMLG2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTG2				00h	0Fh
35h	PWMLH0	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTH0				00h	0Fh
36h	PWMLH1	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTH1				00h	0Fh
37h	PWMLH2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	PWMLOWOUTH2				00h	0Fh
40h	OUTEN0	**RESERVED**	ENOUTB2	ENOUTB1	ENOUTB0	**RESERVED**	ENOUTA2	ENOUTA1	ENOUTA0	00h	77h
41h	OUTEN1	**RESERVED**	ENOUTD2	ENOUTD1	ENOUTD0	**RESERVED**	ENOUTC2	ENOUTC1	ENOUTC0	00h	77h
42h	OUTEN2	**RESERVED**	ENOUTF2	ENOUTF1	ENOUTF0	**RESERVED**	ENOUTE2	ENOUTE1	ENOUTE0	00h	77h

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ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default	EEPROM default
43h	OUTEN3	**RESERVED**	**ENOUTH2**	ENOUTH1	ENOUTH0	**RESERVED**	ENOUTG2	ENOUTG1	ENOUTG0	00h	77h
44h	PWMSHARE	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	SHAREPWM				00h	00h
50h	IOUTA0	**RESERVED**	**RESERVED**	IOUTA0						EEPROM	3Fh
51h	IOUTA1	**RESERVED**	**RESERVED**	IOUTA1						EEPROM	3Fh
52h	IOUTA2	**RESERVED**	**RESERVED**	IOUTA2						EEPROM	3Fh
53h	IOUTB0	**RESERVED**	**RESERVED**	IOUTB0						EEPROM	3Fh
54h	IOUTB1	**RESERVED**	**RESERVED**	IOUTB1						EEPROM	3Fh
55h	IOUTB2	**RESERVED**	**RESERVED**	IOUTB2						EEPROM	3Fh
56h	IOUTC0	**RESERVED**	**RESERVED**	IOUTC0						EEPROM	3Fh
57h	IOUTC1	**RESERVED**	**RESERVED**	IOUTC1						EEPROM	3Fh
58h	IOUTC2	**RESERVED**	**RESERVED**	IOUTC2						EEPROM	3Fh
59h	IOUTD0	**RESERVED**	**RESERVED**	IOUTD0						EEPROM	3Fh
5Ah	IOUTD1	**RESERVED**	**RESERVED**	IOUTD1						EEPROM	3Fh
5Bh	IOUTD2	**RESERVED**	**RESERVED**	IOUTD2						EEPROM	3Fh
5Ch	IOUTE0	**RESERVED**	**RESERVED**	IOUTE0						EEPROM	3Fh
5Dh	IOUTE1	**RESERVED**	**RESERVED**	IOUTE1						EEPROM	3Fh
5Eh	IOUTE2	**RESERVED**	**RESERVED**	IOUTE2						EEPROM	3Fh
5Fh	IOUTF0	**RESERVED**	**RESERVED**	IOUTF0						EEPROM	3Fh
60h	IOUTF1	**RESERVED**	**RESERVED**	IOUTF1						EEPROM	3Fh
61h	IOUTF2	**RESERVED**	**RESERVED**	IOUTF2						EEPROM	3Fh
62h	IOUTG0	**RESERVED**	**RESERVED**	IOUTG0						EEPROM	3Fh
63h	IOUTG1	**RESERVED**	**RESERVED**	IOUTG1						EEPROM	3Fh
64h	IOUTG2	**RESERVED**	**RESERVED**	IOUTG2						EEPROM	3Fh
65h	IOUTH0	**RESERVED**	**RESERVED**	IOUTH0						EEPROM	3Fh
66h	IOUTH1	**RESERVED**	**RESERVED**	IOUTH1						EEPROM	3Fh
67h	IOUTH2	**RESERVED**	**RESERVED**	IOUTH2						EEPROM	3Fh
6Ah	LOWBAT	**RESERVED**	LOWVBATTH[6:0]							EEPROM	00h

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ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default	EEPROM default
6Bh	CONF_FD1	AUTOSS	LOWVBAT_FD	OPENTH	DISRETRY	PSθ[1:0]		OFFDelay	OFFOUT_FD	EEPROM	00h
6Ch	CONF_FD2	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	EEPROM	00h
70h	DIAGEN0	**RESERVED**	DIAGEN OUTB2	DIAGEN OUTB1	DIAGEN OUTB0	**RESERVED**	DIAGEN OUTA2	DIAGEN OUTA1	DIAGEN OUTA0	EEPROM	77h
71h	DIAGEN1	**RESERVED**	DIAGEN OUTD2	DIAGEN OUTD1	DIAGEN OUTD0	**RESERVED**	DIAGEN OUTC2	DIAGEN OUTC1	DIAGEN OUTC0	EEPROM	77h
72h	DIAGEN2	**RESERVED**	DIAGEN OUTF2	DIAGEN OUTF1	DIAGEN OUTF0	**RESERVED**	DIAGEN OUTE2	DIAGEN OUTE1	DIAGEN OUTE0	EEPROM	77h
73h	DIAGEN3	**RESERVED**	DIAGEN OUTH2	DIAGEN OUTH1	DIAGEN OUTH0	**RESERVED**	DIAGEN OUTG2	DIAGEN OUTG1	DIAGEN OUTG0	EEPROM	77h
74h	SLSTHSEL0	**RESERVED**	SLSTHOUTB2	SLSTHOUTB1	SLSTHOUTB0	**RESERVED**	SLSTHOUTA2	SLSTHOUTA1	SLSTHOUTA0	EEPROM	00h
75h	SLSTHSEL1	**RESERVED**	SLSTHOUTD2	SLSTHOUTD1	SLSTHOUTD0	**RESERVED**	SLSTHOUTC2	SLSTHOUTC1	SLSTHOUTC0	EEPROM	00h
76h	SLSTHSEL2	**RESERVED**	SLSTHOUTF2	SLSTHOUTF1	SLSTHOUTF0	**RESERVED**	SLSTHOUTE2	SLSTHOUTE1	SLSTHOUTE0	EEPROM	00h
77h	SLSTHSEL3	**RESERVED**	SLSTHOUTH2	SLSTHOUTH1	SLSTHOUTH0	**RESERVED**	SLSTHOUTE2	SLSTHOUTG1	SLSTHOUTG0	EEPROM	00h
78h	SLSDAC0	**RESERVED**	SLSTH0							EEPROM	00h
79h	SLSDAC1	**RESERVED**	SLSTH1							EEPROM	00h
7Ah	REFERENCE	SLSEN	REFRANGE		LOWVSTH					EEPROM	60h
7Bh	DIAG	IRETRY				BLANK				EEPROM	00h
7Ch	DIAGMASK	MASKLOWSUP	MASKVSUV	MASKREF	MASKPRETSD	MASKTSD	MASKMTPCRC	**RESERVED**	**RESERVED**	EEPROM	00h
7Dh	OUTMASK	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	MASKOPEN	MASKSHORT	MASKSLS	EEPROM	00h
7Eh	DIM	EXPEN	PSEN	12BIT	PSMEN	PWMFREQ				EEPROM	30h
80h	FSMAP0	**RESERVED**	FSOUTB2	FSOUTB1	FSOUTB0	**RESERVED**	FSOUTA2	FSOUTA1	FSOUTA0	EEPROM	00h
81h	FSMAP1	**RESERVED**	FSOUTD2	FSOUTD1	FSOUTD0	**RESERVED**	FSOUTC2	FSOUTC1	FSOUTC0	EEPROM	00h
82h	FSMAP2	**RESERVED**	FSOUTF2	FSOUTF1	FSOUTF0	**RESERVED**	FSOUTE2	FSOUTE1	FSOUTE0	EEPROM	00h
83h	FSMAP3	**RESERVED**	FSOUTH2	FSOUTH1	FSOUTH0	**RESERVED**	FSOUTG2	FSOUTG1	FSOUTG0	EEPROM	00h
84h	FLEXWIRE0	WDTIMER				DBWTIMER			ACKEN	EEPROM	01h
85h	FLEXWIRE1	**RESERVED**	**RESERVED**	DEVADDR [4]	EXTADDR	DEVADDR				EEPROM	10h
86h	FLEXWIRE2	**RESERVED**	**RESERVED**	**RESERVED**	OFAF	INITTIMER				EEPROM	10h

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ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default	EEPROM default
87h	CRC	MTPCRC								EEPROM	B0h[1]

ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
90h	ADCCH	**RESERVED**	**RESERVED**	**RESERVED**	ADCCHSEL					00h
91h	CLR	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	CLRFS	CLRFAULT	CLRPOR	00h
92h	DEBUG	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	FORCEFS	FORCEERR	00h
93h	LOCK	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	BRTLOCK	CONFLOCK	IOUTLOCK	03h
94h	CLRREG	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	SOFTRESET	EEPLOAD	REGDEFAULT	00h
95h	CTRL-R	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	00h
96h	CTRLGATE	CTRLGATE								00h
97h	EEP	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	EEPPROG	EEPMODE	00h
98h	EEPGATE	EEPGATE								00h
A0h	FLAG_ERR	FLAG_LOWSUP	FLAG_VSUV	FLAG_REF	FLAG_PRETSD	FLAG_TSD	FLAG_EEPCRC	FLAG_OUT	FLAG_ERR	01h
A1h	FLAG_STATUS	**RESERVED**	FLAG_EXTFS1	FLAG_EXTFS0	FLAG_PROGDONE	FLAG_FS	FLAG_ADCDONE	FLAG_ADCERR	FLAG_POR	01h
A2h	FLAG_ADC	ADC_OUT								00h
A3h	FLAG_SLS0	**RESERVED**	FLAG_ SLSOUTB2	FLAG_ SLSOUTB1	FLAG_ SLSOUTB0	**RESERVED**	FLAG_ SLSOUTA2	FLAG_ SLSOUTA1	FLAG_ SLSOUTA0	00h
A4h	FLAG_SLS1	**RESERVED**	FLAG_ SLSOUTD2	FLAG_ SLSOUTD1	FLAG_ SLSOUTD0	**RESERVED**	FLAG_ SLSOUTC2	FLAG_ SLSOUTC1	FLAG_ SLSOUTC0	00h
A5h	FLAG_SLS2	**RESERVED**	FLAG_ SLSOUTF2	FLAG_ SLSOUTF1	FLAG_ SLSOUTF0	**RESERVED**	FLAG_ SLSOUTE2	FLAG_ SLSOUTE1	FLAG_ SLSOUTE0	00h
A6h	FLAG_SLS3	**RESERVED**	FLAG_ SLSOUTH2	FLAG_ SLSOUTH1	FLAG_ SLSOUTH0	**RESERVED**	FLAG_ SLSOUTG2	FLAG_ SLSOUTG1	FLAG_ SLSOUTG0	00h
A7h	FLAG_OPEN0	**RESERVED**	FLAG_ OPENOUTB2	FLAG_ OPENOUTB1	FLAG_ OPENOUTB0	**RESERVED**	FLAG_ OPENOUTA2	FLAG_ OPENOUTA1	FLAG_ OPENOUTA0	00h
A8h	FLAG_OPEN1	**RESERVED**	FLAG_ OPENOUTD2	FLAG_ OPENOUTD1	FLAG_ OPENOUTD0	**RESERVED**	FLAG_ OPENOUTC2	FLAG_ OPENOUTC1	FLAG_ OPENOUTC0	00h
A9h	FLAG_OPEN2	**RESERVED**	FLAG_ OPENOUTF2	FLAG_ OPENOUTF1	FLAG_ OPENOUTF0	**RESERVED**	FLAG_ OPENOUTE2	FLAG_ OPENOUTE1	FLAG_ OPENOUTE0	00h

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ADDR	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Default
AAh	FLAG_OPEN3	**RESERVED**	FLAG_ OPENOUTH2	FLAG_ OPENOUTH1	FLAG_ OPENOUTH0	**RESERVED**	FLAG_ OPENOUTG2	FLAG_ OPENOUTG1	FLAG_ OPENOUTG0	00h
ABh	FLAG_SHORT0	**RESERVED**	FLAG_ SHORTOUTB2	FLAG_ SHORTOUTB1	FLAG_ SHORTOUTB0	**RESERVED**	FLAG_ SHORTOUTA2	FLAG_ SHORTOUTA1	FLAG_ SHORTOUTA0	00h
ACh	FLAG_SHORT1	**RESERVED**	FLAG_ SHORTOUTD2	FLAG_ SHORTOUTD1	FLAG_ SHORTOUTD0	**RESERVED**	FLAG_ SHORTOUTC2	FLAG_ SHORTOUTC1	FLAG_ SHORTOUTC0	00h
ADh	FLAG_SHORT2	**RESERVED**	FLAG_ SHORTOUTF2	FLAG_ SHORTOUTF1	FLAG_ SHORTOUTF0	**RESERVED**	FLAG_ SHORTOUTE2	FLAG_ SHORTOUTE1	FLAG_ SHORTOUTE0	00h
AEh	FLAG_SHORT3	**RESERVED**	FLAG_ SHORTOUTH2	FLAG_ SHORTOUTH1	FLAG_ SHORTOUTH0	**RESERVED**	FLAG_ SHORTOUTG2	FLAG_ SHORTOUTG1	FLAG_ SHORTOUTG0	00h
AFh	FLAG_EEPCRC	CALC_EEPCRC								00h
B0h	FLAG_CONFCRC	CALC_CONFCRC								00h
B1h	FLAG_FD	**RESERVED**	**RESERVED**	**RESERVED**	FLAG_LOWVBAT	FLAG_ECC	FLAG_CMP	FLAG_OFFOUT	FLAG_LDOOV	00h
B2h	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	**RESERVED**	00h
B3h	ADC_IREF	ADC_IREF								00h

[1] Factory default value; subsequent calculations follow the MTPCRC formula.

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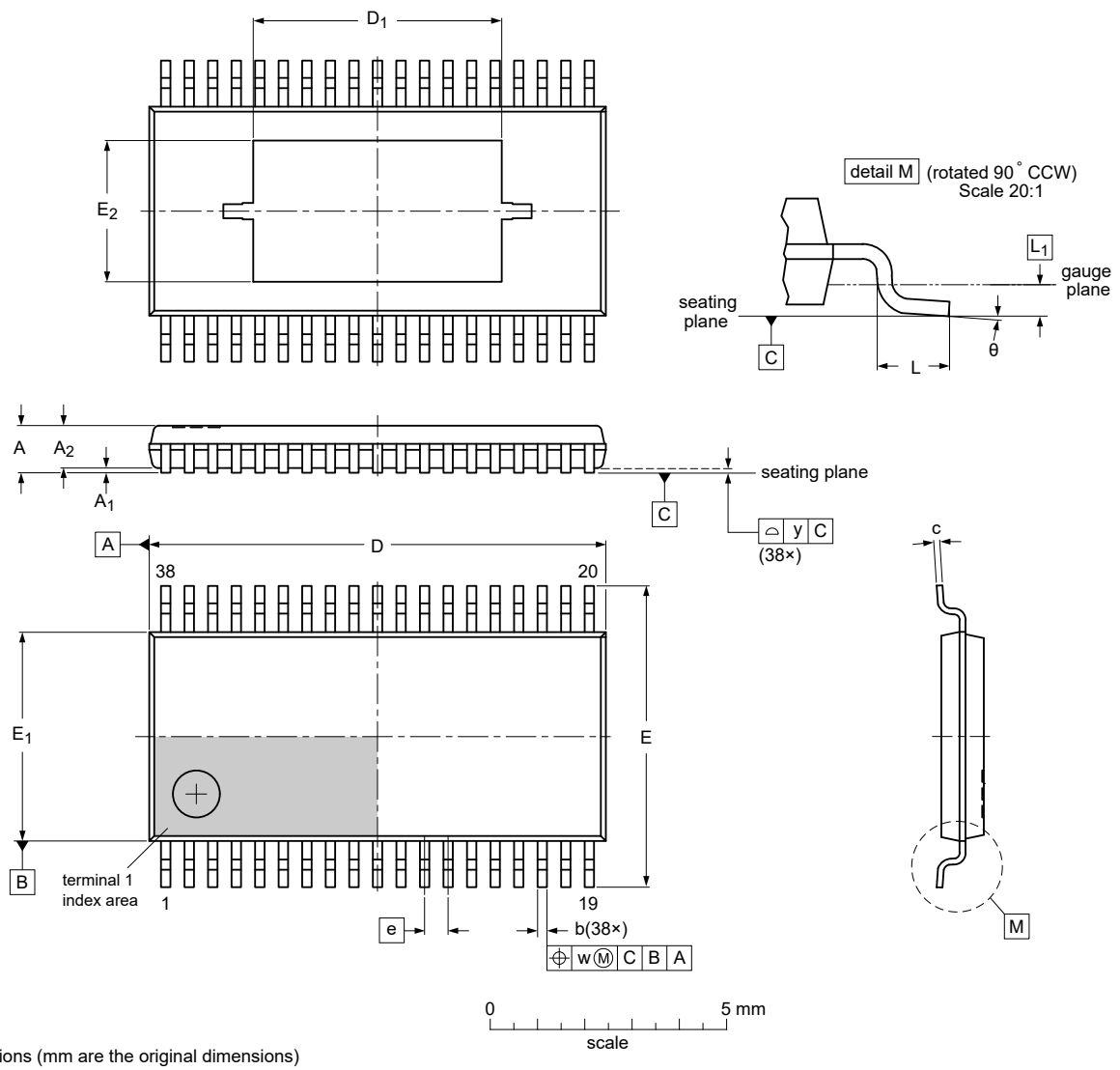
16. Package outline

**plastic, thermal enhanced thin shrink small outline package;
38 leads; 0.5mm pitch; 9.7mm × 4.4mm × 1.2mm body** **SOT8106-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	D_1	E	E_1	E_2	e	L	L_1	w	y	θ
mm	max	1.20	0.15	1.05	0.27	0.20	9.80	5.38	6.60	4.50	3.10	0.50 BSC	0.75	0.25 BSC	0.08	0.05	8°
	nom																
	min		0.05	0.80	0.17	0.09	9.60	5.18	6.20	4.30	2.90		0.45				0°

Note

1. Dimension D does not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burr shall not exceed 0.15 mm per end. Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

sot8106-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8106-1						25-06-30

Fig. 44. Package outline SOT8106-1 (HTSSOP38)

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17. Abbreviations

Table 31. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
ANSI	American National Standards Institute
ASIL	Automotive Safety Integrity Levels
BCM	Body Control Module
CAN	Controller Area Network
CDM	Charged Device Model
CRC	Cyclic Redundancy Check
DC	Dot Correction
ECC	Error Correction Code
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FS	Fail-Safe
HBM	Human Body Model
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
JEDEC	Joint Electron Device Engineering Council
LED	Light Emitting Diode
MTP	Multi-Time Programming
PCB	Printed Circuit Board
POR	Power-On-Reset
PWM	Pulse-Width Modulation
UART	Universal Asynchronous Receiver/Transmitter
UVLO	Undervoltage Lockout

18. Revision history

Table 32. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX1324X_Q100 v.1.2	20251023	Product data sheet	-	NEX1324X_Q100 v.1.1
Modifications:	• Section 2 and Table 8 updated.			
NEX1324X_Q100 v.1.1	20250929	Product data sheet	-	NEX1324X_Q100 v.1
Modifications:	• The document status changed from Preliminary to Product. • Section 14 added. • Section 2 and Table 6 updated.			
NEX1324X_Q100 v.1	20250825	Preliminary data sheet	-	-

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19. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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