NEX10058

1 A triple-output AMOLED display power supply

Rev. 1.1 — 24 December 2025 Product data sheet

1. General description

NEX10058 is designed for powering AMOLED (Active-Matrix Organic LED) displays which require ELVDD, ELVSS and AVDD.

It integrates a boost converter for ELVDD, an inverting buck-boost converter for ELVSS and a boost converter for AVDD. Output voltages of all the three converters can be programmed in digital steps through the digital interface control pins (ASWIRE and ESWIRE).

The device features high efficiency and excellent line and load regulation and transient performance which are well suited for AMOLED applications and is critical to battery-powered applications supply. It features an enhanced output current capability of up to 1 A with precise output voltage accuracy, resulting in higher brightness and superior display performance for AMOLED screens.

NEX10058 is available in a green WLCSP25 package.

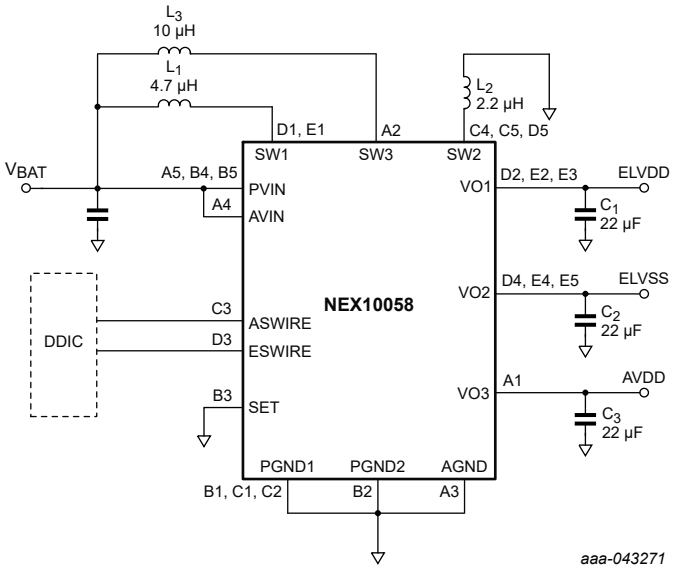


Fig. 1. Typical application circuit

2. Features and benefits

- Input voltage range: 2.5 V to 5.0 V
- Synchronous boost converter (ELVDD)
  - 4.6 V to 5.0 V output voltage with 100 mV steps
  - 4.6 V default output voltage
  - ±0.5% output accuracy
  - V_{IN} ($V_{AVIN;PVIN}$) and V_{OUT} bi-directional isolation
- Synchronous inverting buck-boost converter (ELVSS)
  - -6.6 V to -0.5 V output voltage with 100 mV steps
  - -4.0 V default output voltage
  - ±0.5% output accuracy
  - V_{IN} ($V_{AVIN;PVIN}$) and V_{OUT} bi-directional isolation
- ELVDD-ELVSS combined output current capability:
  - 1 A at V_{IN} ($V_{AVIN;PVIN}$) = 3.2 V; V_{ELVSS} = -5.5 V
  - 1 A at V_{IN} ($V_{AVIN;PVIN}$) = 2.9 V; V_{ELVSS} = -4.0 V
  - 0.8 A at V_{IN} ($V_{AVIN;PVIN}$) = 2.5 V; V_{ELVSS} = -4.0 V
- Synchronous boost converter (AVDD)
  - 7.1 V to 7.8 V output voltage (SET = low) with 100 mV steps
  - 6.9 V to 7.9 V output voltage (SET = high) with 50 mV steps
  - 7.6 V default output voltage
  - ±1% output accuracy
  - 150 mA output current capability
  - V_{IN} ($V_{AVIN;PVIN}$) and V_{OUT} bi-directional isolation
- High switching frequency: 1.45 MHz
- Dual SWIRE interfaces
  - ELVDD/ELVSS and AVDD output voltage programming
  - Output discharge on/off control
  - ELVSS transition time programming
- Excellent line and load transient performance
- UVLO and OTSD protection
- Soft start with inrush current limitation
- Short-circuit protection
- High efficiency at full load range
- 25-ball 1.965 mm x 1.965 mm WLCSP package

3. Applications

- Mobile phones
- Tablets
- Active-Matrix OLED power supply management

4. Ordering information

Table 1. Ordering information

Type number	Temperature range (T_{amb})	Name	Description	Version
NEX10058UNL	-40 °C to 85 °C	WLCSP25	WLCSP25: wafer level chip-size package; 25 bumps	SOT8117

5. Marking

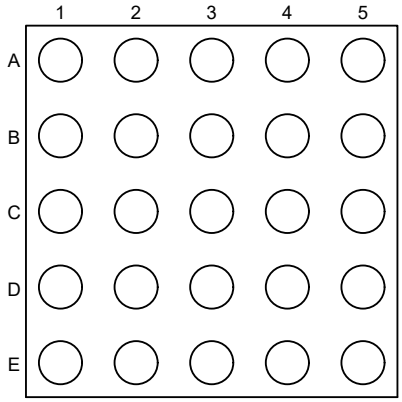
Table 2. Marking code

Type number	Marking code
NEX10058UNL	N10058

6. Pinning information

6.1. Pinning configuration

UNL package
WLCSP25_SOT8117



VO3	SW3	AGND	AVIN	PVIN
PGND1	PGND2	SET	PVIN	PVIN
PGND1	PGND1	ASWIRE	SW2	SW2
SW1	VO1	ESWIRE	VO2	SW2
SW1	VO1	VO1	VO2	VO2

Transparent top view

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6.2. Pin description

Symbol	Pin	I/O	Description
VO3	A1	O	VO3 boost converter output.
PGND1	B1, C1, C2	G	VO1 boost converter power ground.
SW1	D1, E1	I/O	VO1 boost converter switching node.
SW3	A2	I/O	VO3 boost converter switching node.
PGND2	B2	G	VO2 inverting buck-boost converter and VO3 boost converter power ground.
VO1	D2, E2, E3	O	VO1 boost converter output.
AGND	A3	G	Analog ground pin.
SET	B3	I	VO3 output voltage table setting pin.
ASWIRE	C3	I	VO3 boost converter enable control and programming pin. A 170 kΩ pull-down resistor is integrated.
ESWIRE	D3	I	VO1 boost converter and VO2 inverting buck-boost converter enable control and programming pin. A 170 kΩ pull-down resistor is integrated.

Symbol	Pin	I/O	Description
AVIN	A4	I	Analog input supply pin. Keep pin AVIN separated from noises, like pin PWIN.
PVIN	A5, B4, B5	I	Power input supply pin.
SW2	C4, C5, D5	I/O	VO2 inverting buck-boost converter switching node.
VO2	D4, E4, E5	O	VO2 inverting buck-boost converter output.

7. Limiting values

Table 3. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
Pin voltage	AVIN, PVIN, VO1, ASWIRE, SET, ESWIRE, SW1		-0.3	6.0	V
	VO2		-7.0	0.3	V
	VO3, SW3		-0.3	11.0	V
	SW2		-7	6	V
	PGND1, PGND2 to AGND		-0.3	0.3	V
T_{amb}	operating ambient temperature		-40	85	°C
T_j	operating junction temperature		-40	150	°C
T_{stg}	storage temperature		-65	150	°C

8. ESD ratings

Table 4. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{esd}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	-	2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	-500	-	500	V

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	WLCSP25_SOT8117	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	58.5	°C/W

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN} [1]	supply voltage		2.5	-	5.0	V
ELVDD boost converter						
L_1	VO1 boost converter inductor		-	4.7	-	µH
C_{IN1}	VO1 boost converter input capacitance		-	22	-	µF
C_{VO1}	VO1 boost converter output capacitance		-	22 x 2	-	µF
ELVSS inverting buck-boost converter						
L_2	VO2 inverting buck-boost converter inductor		-	2.2	-	µH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN2}	VO2 inverting buck-boost converter input capacitance		-	22	-	µF
C_{VO2}	VO2 inverting buck-boost converter output capacitance		-	22 x 2	-	µF
AVDD converter						
L_3	VO3 boost converter inductor		-	10	-	µH
C_{IN3}	VO3 boost converter input capacitance		-	22	-	µF
C_{VO3}	VO3 boost converter output capacitance		-	10 x 2	-	µF
T_{amb}	operating ambient temperature		-40	-	85	°C
T_j	operating junction temperature		-40	-	125	°C

[1] $V_{IN} = V_{AVIN} = V_{PVIN}$; hereinafter referred to as V_{IN}.

11. Electrical characteristics

Table 7. Electrical characteristics

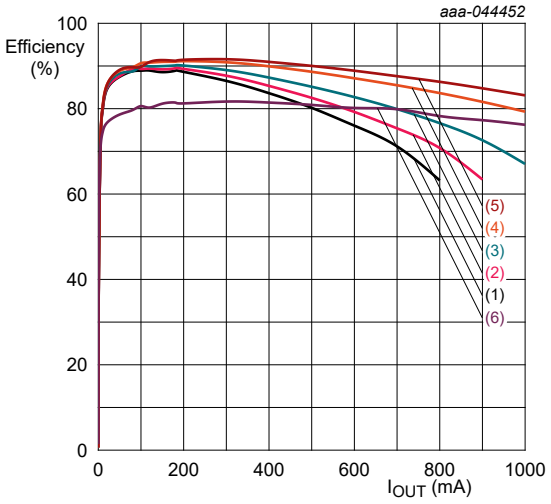
V_{AVIN} = V_{PVIN} = 3.7 V; V_{ESWIRE} = V_{ASWIRE} = V_{AVIN} = V_{PVIN}; V_{VO1} = 4.6 V, V_{VO2} = -4 V; V_{VO3} = 7.6 V; T_{amb} = T_j. Typical values are at T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ	Max	
Supply						
V_{IN}	AVIN, PVIN supply voltage range		2.5	3.7	5.0	V
V_{UVLO}	undervoltage lockout threshold	V_{IN} rising	2.25	2.35	2.45	V
		V_{IN} falling	2.05	2.15	2.25	V
		hysteresis	-	200	-	mV
I_q	quiescent current	no switching	-	1	1.5	mA
		no load	-	3	-	mA
I_{sd}	shutdown current	V_{ESWIRE} = V_{ASWIRE} = 0 V	-	1	2	µA
T_{sd}	thermal shutdown		-	145	-	°C
T_{sd_hys}	thermal shutdown hysteresis	retry	-	30	-	°C
ELVDD boost converter (VO1)						
V_{VO1}	VO1 boost converter output		4.6	4.6	5.0	V
V_{VO1_step}	VO1 boost converter output step	digital adjust step	-	100	-	mV
t_{SS1}	VO1 soft start time		-	1.6	2	ms
V_{VO1_acc}	VO1 boost converter output accuracy	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; no load; T_{amb} = 25 °C	-0.5%	-	0.5%	-
		V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; no load	±0.8%	-	0.7%	-
$V_{VO1\_linereg}$	line regulation	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; 100 mA	-	2	-	mV
$V_{VO1\_loadreg}$	load regulation	1 mA ≤ I_{VO1} ≤ 1 A	-	10	-	mV
I_{SW1_lim}	SW1 valley current limit	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V	1.9	2.2	2.5	A
f_{SW}	switching frequency		-	1.45	-	MHz
$R_{DS-ON-LS}$	low-side MOSFET ON-resistance			95	-	mΩ
$R_{DS-ON-HS}$	high-side MOSFET ON-resistance		-	95	-	mΩ
V_{SCP}	short-circuit protection	V_{VO1} falling	-	90%	-	-
t_{SCP}	SCP deglitch time		-	1	-	ms
R_{DIS_VO1}	discharging Resistance	ESWIRE = low; discharge on	-	35	-	Ω
ELVSS buck-boost converter (VO2: PSM)						
V_{VO2}	VO2 inverting buck-boost converter output		-6.6	-4.0	-0.5	V
V_{VO2_step}	VO2 inverting buck-boost converter output step	digital adjust step	-	100	-	mV
t_{trans}	VO2 transition time	fast transition, default	-	60	-	µs/100 mV
		slow transition, SWIRE control	-	16	-	ms/100 mV
t_{SS2}	VO2 soft start time		-	1	2	ms
t_{DELAY}	VO2 start-up time delay after VO1 starts to ramp		-	10	-	ms

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 85 °C			Unit
			Min	Typ	Max	
V_{VO2_acc}	VO2 inverting buck-boost output accuracy	V_{VO2} = -4 V; no load; T_{amb} = 25 °C	-25	-	25	mV
		V_{VO2} = -4 V; no load	-40	-	40	mV
$V_{VO2\_linereg}$	line regulation	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; 100 mA	-	2	-	mV
$V_{VO2\_loadreg}$	load regulation	1 mA ≤ I_{VO1} ≤ 1 A	-	10	-	mV
I_{SW2_lim}	SW2 current limit	V_{AVIN} = V_{PVIN} = 2.7 V to 5 V	3.8	4.5	5.5	A
f_{SW}	switching frequency		-	1.45	-	MHz
$R_{DS-ON-LS}$	low-side MOSFET ON-resistance		-	35	-	mΩ
$R_{DS-ON-HS}$	high-side MOSFET ON-resistance		-	80	-	mΩ
V_{SCP}	short-circuit protection	VO2 falling	-	80%	-	-
t_{SCP}	SCP deglitch time		-	1	-	ms
R_{DIS_VO2}	discharging resistance	ESWIRE = low; discharge on	-	40	-	Ω
AVDD boost converter (VO3: PCM, PSM)						
V_{VO3}	VO3 boost converter output	SET = low	7.1	7.6	7.8	V
		SET = high	6.9	7.6	7.9	V
V_{VO3_step}	VO3 boost converter output step	SET = low	-	100	-	mV
		SET = high	-	50	-	mV
t_{SS3}	VO3 soft start time		-	2	4	ms
V_{VO3_acc}	VO3 boost converter output variation	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; I_{VO3} = 0 mA to 150 mA; T_{amb} = 25 °C	-0.8%	-	0.8%	-
		V_{AVIN} = V_{PVIN} = 2.5 V to 5 V; I_{VO3} = 0 mA to 150 mA	-1%	-	1%	-
I_{SW3_lim}	SW3 current limit	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V	0.8	1.1	1.4	A
f_{SW}	switching frequency		-	1.45	-	MHz
$R_{DS-ON-LS}$	low-side MOSFET ON-resistance		-	190	-	mΩ
$R_{DS-ON-HS}$	high-side MOSFET ON-resistance		-	700	-	mΩ
V_{SCP}	short-circuit protection	V_{VO3} falling	-	90%	-	V
t_{SCP}	SCP deglitch time		-	1	-	ms
R_{DIS_VO3}	discharging resistance	ASWIRE = low; discharge on	-	40	-	Ω
SWIRE interface						
R_{pd}	pull-down resistor	ASWIRE	-	170	-	kΩ
		ESWIRE	-	170	-	kΩ
V_{IH}	ASWIRE/ESWIRE logic input high threshold voltage	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V	0.84	-	-	V
V_{IL}	ASWIRE/ESWIRE logic input low threshold voltage	V_{AVIN} = V_{PVIN} = 2.5 V to 5 V	-	-	0.4	V
t_{INIT}	initialization time		500	-	-	µs
t_H	ASWIRE/ESWIRE logic input high time		2	10	20	µs
t_L	ASWIRE/ESWIRE logic input low time		2	10	20	µs
t_{sd}	shutdown time		35	45	55	µs
t_{STORE}	data storage time		35	45	55	µs

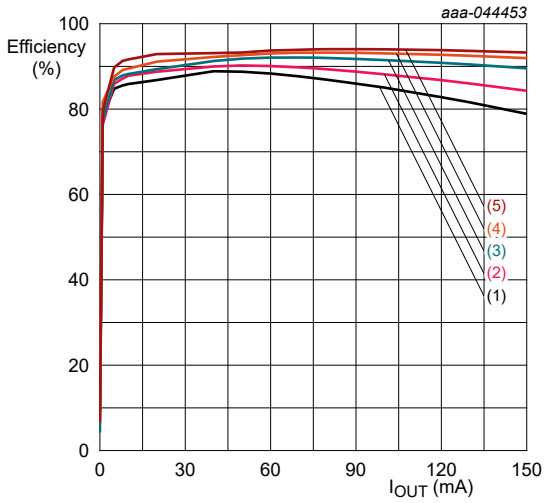
12. Typical characteristics

Table 8. Typical characteristics



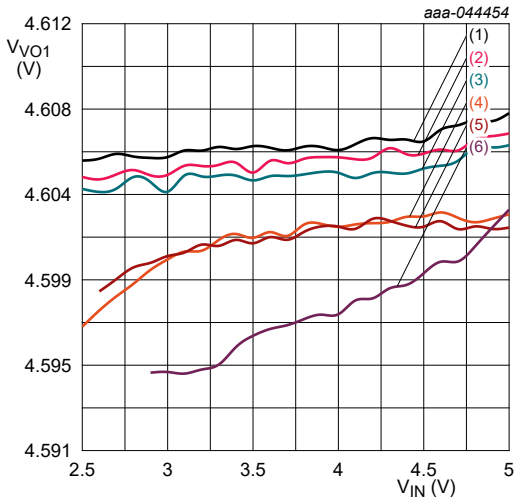
V_{VO1} = 4.6 V; V_{VO2} = -4 V
(1) V_{IN} = 2.5 V
(2) V_{IN} = 2.7 V
(3) V_{IN} = 3 V
(4) V_{IN} = 3.7 V
(5) V_{IN} = 4.2 V
(6) V_{IN} = 5 V

Fig. 2. VO1 and VO2 combined efficiency versus output current



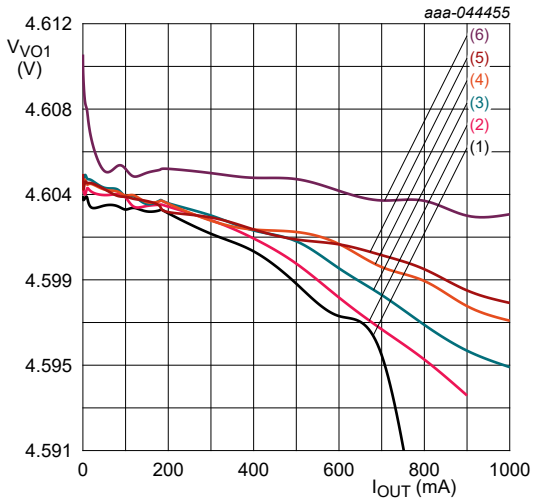
V_{VO3} = 7.6 V
(1) V_{IN} = 2.5 V
(2) V_{IN} = 2.9 V
(3) V_{IN} = 3.7 V
(4) V_{IN} = 4.4 V
(5) V_{IN} = 5 V

Fig. 3. VO3 efficiency versus output current



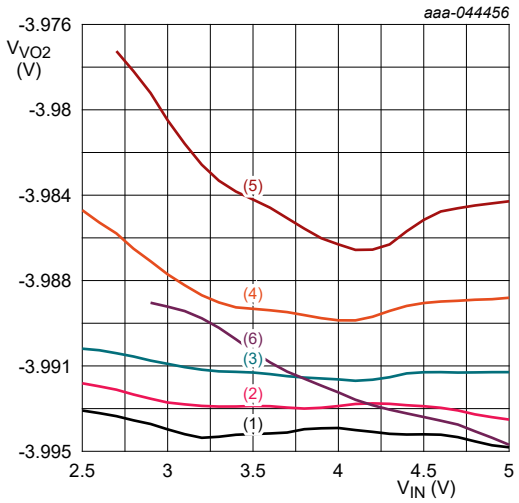
V_{VO1} = 4.6 V
(1) I_{OUT} = 0 mA
(2) I_{OUT} = 100 mA
(3) I_{OUT} = 300 mA
(4) I_{OUT} = 600 mA
(5) I_{OUT} = 850 mA
(6) I_{OUT} = 1000 mA

Fig. 4. VO1 line regulation



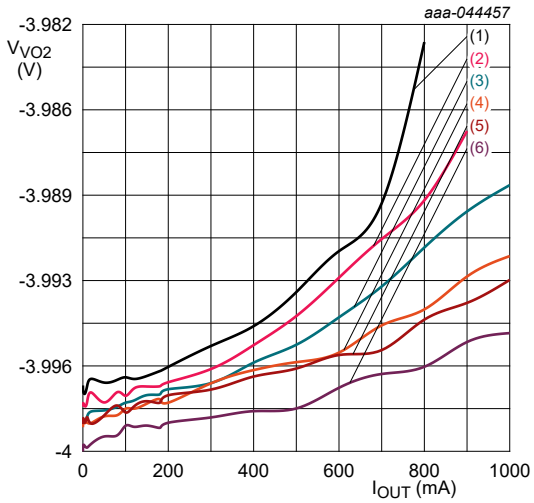
V_{VO1} = 4.6 V
(1) V_{IN} = 2.5 V
(2) V_{IN} = 2.7 V
(3) V_{IN} = 3 V
(4) V_{IN} = 3.7 V
(5) V_{IN} = 4.2 V
(6) V_{IN} = 5 V

Fig. 5. VO1 load regulation



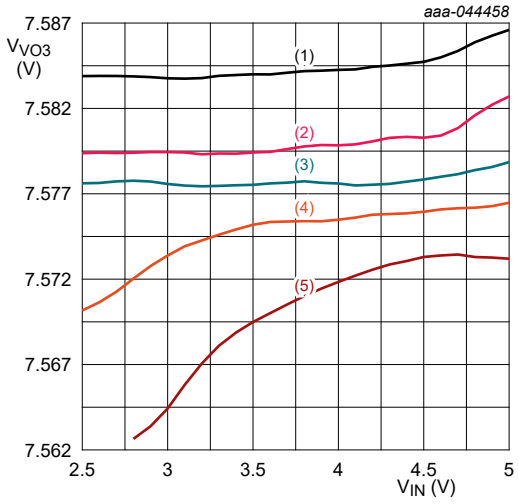
V_{VO2} = -4 V
(1) I_{OUT} = 0 mA
(2) I_{OUT} = 100 mA
(3) I_{OUT} = 300 mA
(4) I_{OUT} = 600 mA
(5) I_{OUT} = 850 mA
(6) I_{OUT} = 1000 mA

Fig. 6. VO2 line regulation



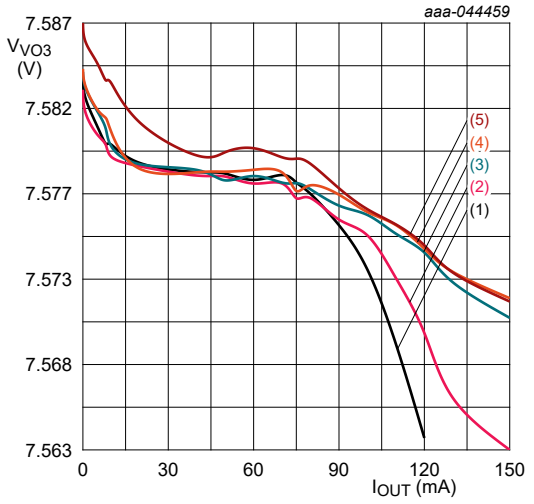
V_{VO2} = -4 V
(1) V_{IN} = 2.5 V
(2) V_{IN} = 2.7 V
(3) V_{IN} = 3 V
(4) V_{IN} = 3.7 V
(5) V_{IN} = 4.2 V
(6) V_{IN} = 5 V

Fig. 7. VO2 load regulation



V_{VO3} = 7.6 V
(1) I_{OUT} = 0 mA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 50 mA
(4) I_{OUT} = 75 mA
(5) I_{OUT} = 150 mA

Fig. 8. VO3 line regulation



V_{VO3} = 7.6 V
(1) V_{IN} = 2.5 V
(2) V_{IN} = 2.9 V
(3) V_{IN} = 3.7 V
(4) V_{IN} = 4.4 V
(5) V_{IN} = 5 V

Fig. 9. VO3 load regulation

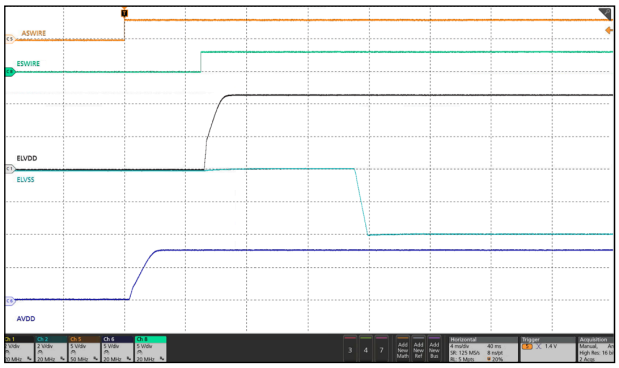


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Fig. 10. Start-up sequence

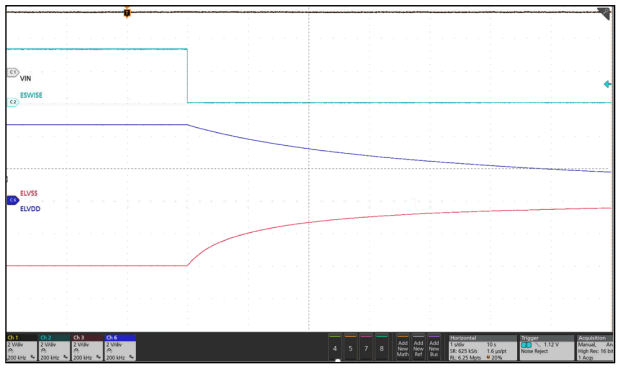

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Fig. 11. Shutdown sequence (discharge = OFF)

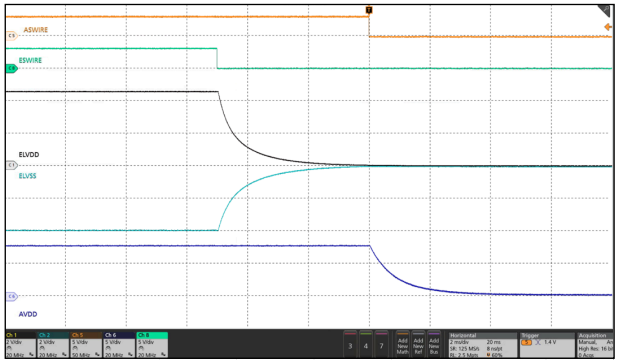

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Fig. 12. Shutdown sequence (discharge = ON)

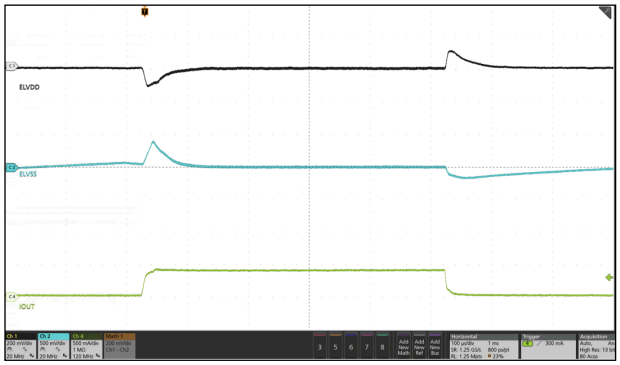

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Fig. 13. VO1 and VO2 load transient (0 mA to 400 mA)

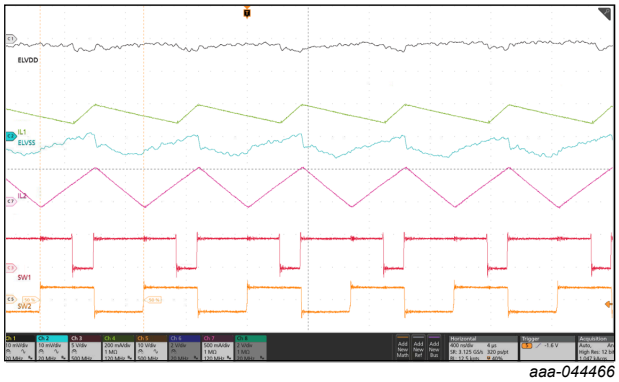

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Fig. 14. VO1 and VO2 output ripple (100 mA)

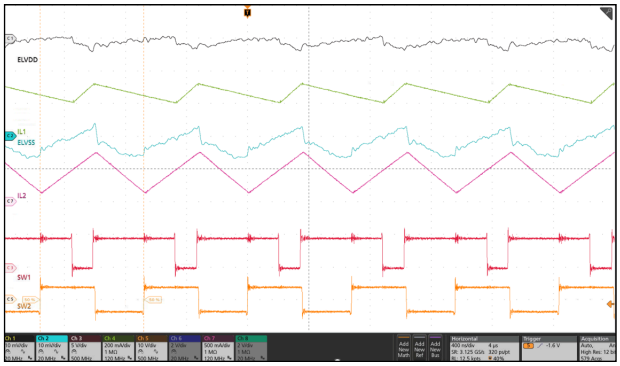

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Fig. 15. VO1 and VO2 output ripple (200 mA)

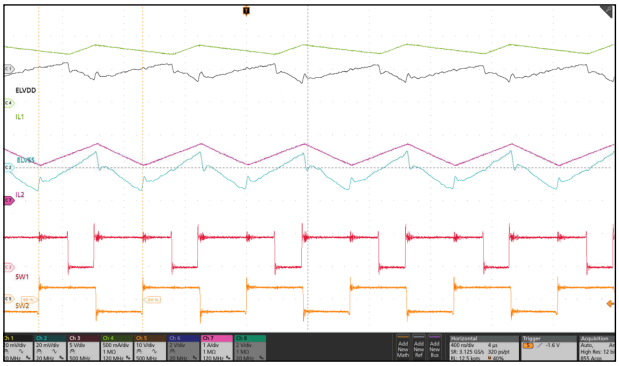

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Fig. 16. VO1 and VO2 output ripple (600 mA)

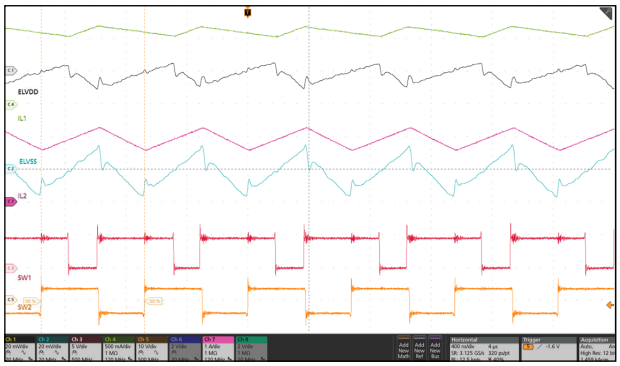

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Fig. 17. VO1 and VO2 output ripple (800 mA)

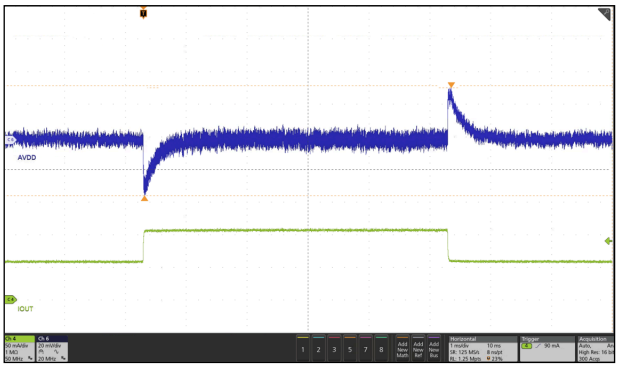

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Fig. 18. VO3 load transient (50 mA to 100 mA)

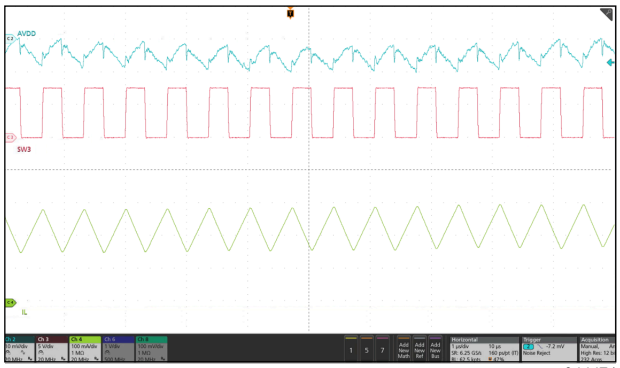

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Fig. 19. VO3 output ripple (100 mA)

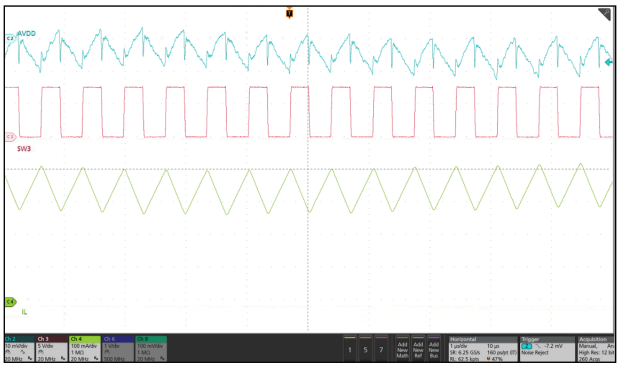

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Fig. 20. VO3 output ripple (150 mA)

13. Detailed description

13.1. Overview

NEX10058 is designed for powering AMOLED (Active-Matrix Organic LED) displays which require ELVDD, ELVSS and AVDD. It integrates a boost converter for ELVDD, an inverting buck-boost converter for ELVSS and a boost converter for AVDD. Output voltages of all the three converters can be programmed in digital steps through the digital interface control pins (ASWIRE and ESWIRE).

13.2. Functional block diagram

The NEX10058 functional block diagram is shown in Fig. 21.

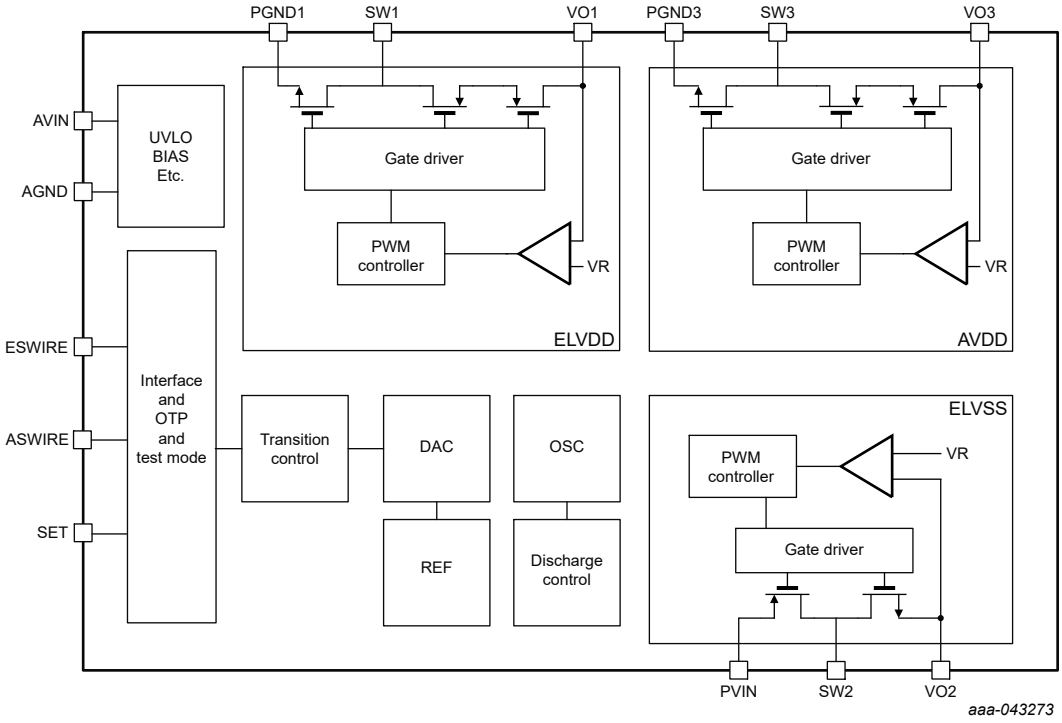


Fig. 21. Functional block diagram

13.3. Feature description

13.3.1. Undervoltage lockout (UVLO)

NEX10058 integrates an undervoltage lockout block (UVLO) that enables the device once the voltage on the V_{IN} pin exceeds the UVLO threshold. No output voltage will be generated if the enable signals are not pulled high. The device, as well as all converters (ELVDD, ELVSS, AVDD), will be disabled as soon as the V_{IN} voltage falls below the UVLO threshold.

The UVLO threshold is designed with a hysteresis, NEX10058 will continue operating as long as V_{IN} voltage stays above 2.25 V. This guarantees a proper operation even in the event of extensive line transients when the battery gets suddenly heavily loaded.

13.3.2. Thermal shutdown (TSD)

The device has a build-in temperature sensor which monitors the internal junction temperature. When the junction temperature exceeds 145 °C, NEX10058 will shut down. When the junction temperature falls below the thermal recovery temperature, approximately 115 °C, the device restarts by using soft-start sequence.

13.3.3. Boost converter (VO1: ELVDD)

Start-up

After V_{IN} voltage rises above UVLO threshold and ESWIRE pulls high, the ELVDD boost regulator will start to work. There is always a soft-start process during start-up procedure to prevent inrush current.

Steady state

The ELVDD boost regulator uses the constant frequency (1.45 MHz fixed) valley current mode topology to ensure reliable over-current protection and fast transient responses. The main switch turns off at the beginning of each clock cycle and the switch current is sensed.

The sensed voltage and a fixed external ramp used to compare with the output voltage of the error amplifier to generate the duty cycle in the PWM modulator. Then the main switch will be turned on and the rectifier switch will turn off until the arrival of the next clock cycle.

The output voltage V_{VO1} is adjustable between 4.6 V and 5 V with a default voltage of 4.6 V with 100 mV step through the ESWIRE pin.

Shutdown

When V_{IN} voltage falls below UVLO threshold or ESWIRE is pulled low, the ELVDD boost regulator will starts to shutdown mode, and there is a discharge function to quickly remove ELVDD voltage after shutdown. To enter shutdown mode, make sure ESWIER voltage keeps low for t_{OFF} time of 45 µs (typical).

In shutdown mode, its output is fully isolated (input to output and output to input).

13.3.4. Inverting buck-boost converter (VO2: ELVSS)

Start-up

After V_{IN} voltage rises above UVLO threshold and ESWIRE pulls high and ELVDD starts soft-start process, and then wait for 10 ms of delay, the ELVSS inverting buck-boost regulator will start to work. The regulator works in peak current mode at the entire start-up procedure.

There is always a soft-start process during start-up procedure to prevent inrush current.

Steady state

The inverting buck-boost converter VO2 operates with a peak-current-mode topology and fixed 1.45 MHz frequency. The VO2 output voltage can be programmed between -6.6 V to -0.5 V (default -4.0 V) with 100 mV steps through the ESWIRE pin.

The ELVSS converter works at PSM mode at light load conditions, which is good for high efficiency.

Shutdown

When V_{IN} falls below UVLO threshold or ESWIRE is pulled low, the inverting Buck-Boost converter VO2 will starts to shutdown mode and there is a discharge option to quickly remove ELVSS voltage after shutdown. To enter shutdown mode, make sure that ESWIER voltage keeps low for t_{OFF} time of 45 µs (typical).

In shutdown mode, its output is fully isolated (input to output and output to input).

13.3.5. Boost converter (VO3: AVDD)

Start-up

After V_{IN} rises above UVLO threshold and ESWIRE pulls high, the ELVDD Boost regulator will start to work. There is always a soft-start process during start-up procedure to prevent inrush current.

Steady state

The AVDD Boost regulator uses the constant frequency (1.45 MHz fixed) peak current mode topology to ensure reliable over-current protection and fast transient responses. The main switch turns on at the beginning of each clock cycle and the switch current is sensed. The sensed voltage and a fixed external ramp used to compare with the output voltage of the error amplifier to generate the duty cycle in the PWM modulator. Then the main switch will be turned off and the rectifier switch will turn on until the arrival of the next clock cycle.

The VO3 output voltage can be programmed through ASWIRE pin, and the output voltage table can be changed by SET pin. When SET = low, the VO3 voltage is available between 7.1 V and 7.8 V (default 7.6 V) with 100 mV steps. While SET = high, the VO3 voltage is available between 6.9 V and 7.9 V (default 7.6 V) with 50 mV steps.

The AVDD converter works at PSM mode at light load conditions, which is good for high efficiency.

Shutdown

When V_{IN} falls below UVLO threshold or ESWIRE is pulled low, the ELVDD Boost regulator will starts to shutdown mode and there is a discharge function to quickly remove ELVDD voltage after shutdown. To enter shutdown mode, make sure ESWIER voltage keeps low for t_{OFF} time of 45 µs (typical).

In shutdown mode, its output is fully isolated (input to output and output to input).

13.3.6. Start-up sequence, soft start, shut-down and discharge

Pulling ASWIRE high enables the VO3 boost converter. Pulling ESWIRE high enables the VO1 boost converter and VO2 buck-boost converter. The VO2 always starts 10 ms later than VO1 with a default value of -4 V. All converters start with soft-start function to limit the inrush current.

VO1, VO2 start-up and programming (ESWIRE)

The ESWIRE interface controls the on/off state of ELVDD and ELVSS. The ELVDD boost converter begins soft start to its default voltage 4.6 V with a t_{INIT} time delay after the ESWIRE logic level goes high. The ELVSS inverting buck-boost converter with -4 V default value starts to operate 10 ms later than the ELVDD boost converter. Both converters are implemented with soft start to limit the inrush current. When ESWIRE interface goes low for t_{OFF} time, the ELVDD and ELVSS converters stop operation simultaneously.

The ELVDD and ELVSS output voltage both are programmable by applying different pulses to ESWIRE interface, which also counts the rise edges, plus a high logic level of ESWIRE lasts longer than a t_{STORE} time is detected after control pulses stop, the ELVDD and ELVSS outputs start altering to the target voltage.

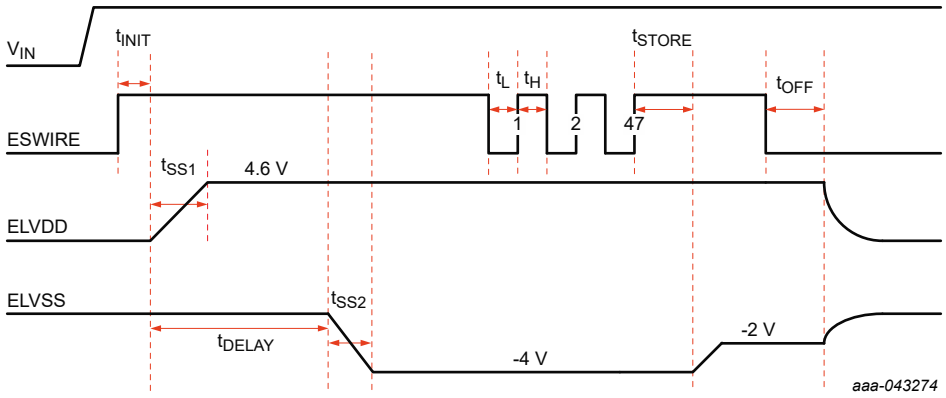


Fig. 22. Power sequence: ELVDD, ELVSS

Table 9. Programming table: ELVDD, ELVSS

ESWIRE pulses	VO2 (ELVSS)	ESWIRE pulses	VO2 (ELVSS)	ESWIRE pulses	VO2 (ELVSS)	ESWIRE pulses	VO1 (ELVDD)
0, default	-4.0 V	22	-4.5 V	44	-2.3 V	0, default	4.6 V
1	-6.6 V	23	-4.4 V	45	-2.2 V	76	5.0 V
2	-6.5 V	24	-4.3 V	46	-2.1 V	77	4.9 V
3	-6.4 V	25	-4.2 V	47	-2.0 V	78	4.8 V
4	-6.3 V	26	-4.1 V	48	-1.9 V	79	4.7 V
5	-6.2 V	27	-4.0 V	49	-1.8 V	80	4.6 V
6	-6.1 V	28	-3.9 V	50	-1.7 V	-	-
7	-6.0 V	29	-3.8 V	51	-1.6 V	-	-
8	-5.9 V	30	-3.7 V	52	-1.5 V	-	-
9	-5.8 V	31	-3.6 V	53	-1.4 V	-	-
10	-5.7 V	32	-3.5 V	54	-1.3 V	-	-
11	-5.6 V	33	-3.4 V	55	-1.2 V	-	-
12	-5.5 V	34	-3.3 V	56	-1.1 V	-	-
13	-5.4 V	35	-3.2 V	57	-1.0 V	-	-
14	-5.3 V	36	-3.1 V	58	-0.9 V	-	-
15	-5.2 V	37	-3.0 V	59	-0.8 V	-	-
16	-5.1 V	38	-2.9 V	60	-0.7 V	-	-
17	-5.0 V	39	-2.8 V	61	-0.6 V	-	-
18	-4.9 V	40	-2.7 V	62	-0.5 V	-	-
19	-4.8 V	41	-2.6 V	-	-	-	-
20	-4.7 V	42	-2.5 V	-	-	-	-
21	-4.6 V	43	-2.4 V	-	-	-	-

Transition timing (ESWIRE)

NEX10058 provides ELVSS transition time control function by ESWIRE command. The transition time is 60 µs in the default fast mode. The device enters slow mode after 74 ESWIRE pulses. The slow mode transition time is 16ms and ELVSS regulates by 4 steps of 25 mV in 16 ms.

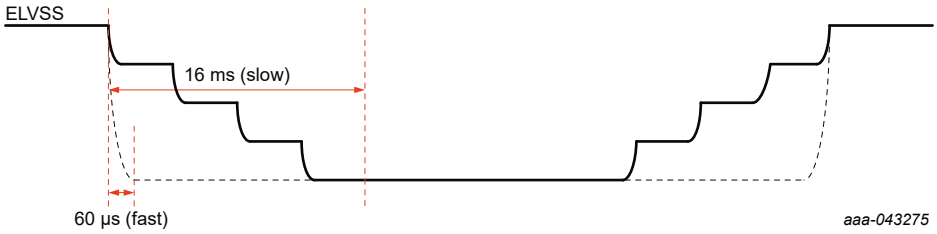


Fig. 23. ELVSS transition timing

Table 10. Transition time: ELVSS

ESWIRE pulses	ELVSS transition time
0, default	60 µs/100 mV
74	16 ms/100 mV
75	60 µs/100 mV

VO3 start-up and programming (ASWIRE)

The AVDD output VO3 can be programmed through ASWIRE interface, and the output voltage table can be changed by the condition of SET interface. When SET = low, AVDD is available from 7.1 V to 7.8 V with 100 mV steps, while SET = high, AVDD is available from 6.9 V to 7.9 V with 50 mV steps.

The AVDD boost converter begins soft start to its default voltage of 7.6 V with a t_{INIT} time delay after the ASWIRE logic level goes high. There is a soft start to limit inrush current.

The AVDD output voltage is programmable by applying different pulses to ASWIRE interface, which counts the rise edges, plus a high logic level to ASWIRE lasts longer than a t_{STORE} time is detected after control pulses stop, AVDD starts adjusting to the target voltage. The AVDD boost converter turns off with a t_{OFF} time delay after the logic level of ASWIRE interface goes from high to low.

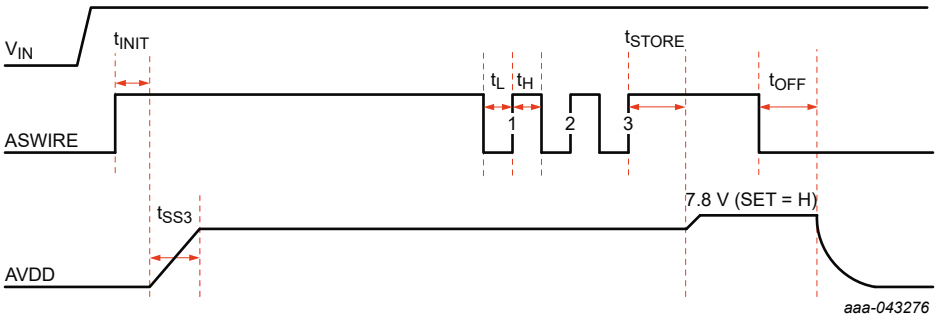


Fig. 24. Power sequence: AVDD

Table 11. Programming table: AVDD

SET = high				SET = low	
ASWIRE pulses	**VO3 (AVDD)**	**ASWIRE pulses**	**VO3 (AVDD)**	**ASWIRE pulses**	**VO3 (AVDD)**
0, default	7.60 V	11	7.40 V	0, default	7.60 V
1	7.90 V	12	7.35 V	1	7.80 V
2	7.85 V	13	7.30 V	2	7.70 V
3	7.80 V	14	7.25 V	3	7.60 V
4	7.75 V	15	7.20 V	4	7.50 V
5	7.70 V	16	7.15 V	5	7.40 V
6	7.65 V	17	7.10 V	6	7.30 V

SET = high				SET = low	
ASWIRE pulses	VO3 (AVDD)	ASWIRE pulses	VO3 (AVDD)	ASWIRE pulses	VO3 (AVDD)
7	7.60 V	18	7.05 V	7	7.20 V
8	7.55 V	19	7.00 V	8	7.10 V
9	7.50 V	20	6.95 V	-	-
10	7.45 V	21	6.90 V	-	-

Fast discharge function

NEX10058 supports fast discharge which is controlled by ASWIRE and SET pins. When power off and the fast discharge is on state, all outputs of the device are discharged to GND. While the fast discharge is off state, all outputs remain Hi-Z status. Table 12 shows the demands of the FD function.

Table 12. Demands of the FD function

SET = high		SET = low	
ASWIRE pulses	Discharge	ASWIRE pulses	Discharge
0, default	Off	0, default	Off
25	On	11	On
26	Off	12	Off

13.3.7. Short-circuit protection (SCP)

The short-circuit protection block monitors the output voltage of AVDD, ELVDD, ELVSS to protect the device of short connections to ground or overload. If the output voltage (AVDD, ELVDD or ELVSS) is lower than the SCP threshold voltage of each over t_{SCP} by overload or output short-circuit condition (including ELVDD short to ELVSS), NEX10058 enters latched shutdown mode, and all converters stop operating.

Only resetting the power supply or both pulling the ASWIRE and ESWIRE interface to low at the same time for more than a t_{OFF} time can restart the device.

Conditions that can trigger SCP:

- During normal operation, AVDD, ELVDD, ELVSS falls below the SCP threshold voltage (90% typical of its nominal value) over t_{SCP}.
- ELVDD is not in regulation for 10 ms after being enabled (ESWIRE = HIGH).
- ELVSS is not in regulation for 10 ms after being enabled (20 ms after ESWIRE = HIGH).
- AVDD is not in regulation 5 ms after being enabled (ASWIRE = HIGH).

13.3.8. Device reset

A power cycle resets all settings to default values as well as the SCP and OTSD.

Conditions that can reset the device:

- Input power cycle to reset all settings to default values.
- SCP and OTSD to reset all settings to default values.
- ASWIRE keeps low for t_{OFF} to reset the voltage of AVDD to default value of 7.6 V, and output discharge configuration.
- ESWIRE keeps low for t_{OFF} to reset the voltage of ELVDD and ELVSS to default value of 4.6 V and -4 V, and ELVSS transition time to default value of fast version.

14. Layout guidelines

- Keep pin AVIN separated from pin PVIN on the ball pins and connected at the far end of the PCB.
- Keep analog ground and power ground connected at a single point.
- Place input capacitors on PVIN and output capacitors on ELVSS as close as possible to the device.
- Place output capacitors on ELVDD and AVDD as close as possible to the device.
- Traces of switching nodes (SW1, SW2 and SW3) should be short and wide.
- Add vias for power paths to obtain lower equivalent resistance on power paths and facilitate heat dissipation.

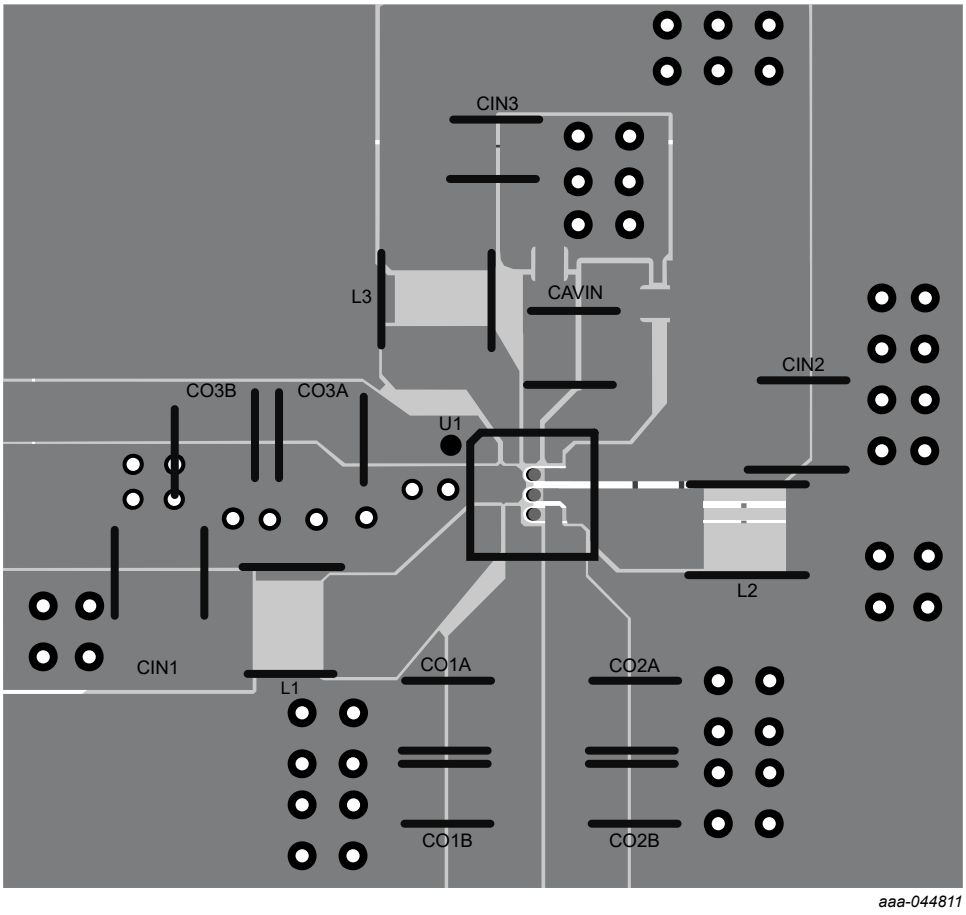
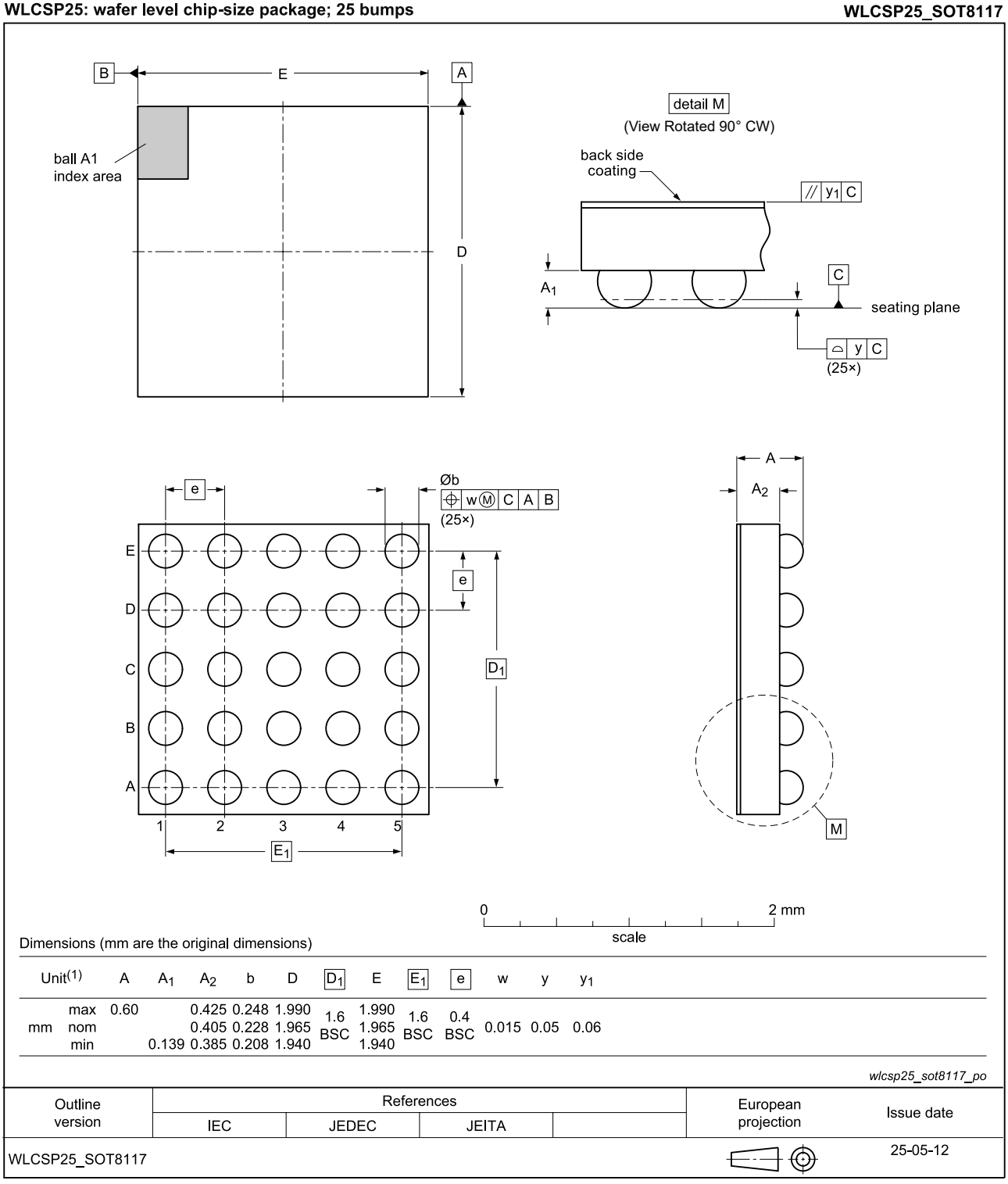


Fig. 25. PCB layout

15. Package outline

WLCSP25: wafer level chip-size package; 25 bumps **WLCSP25_SOT8117**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	b	D	D_1	E	E_1	e	w	y	y_1
mm	max	0.60		0.425	0.248	1.990	1.6 BSC	1.990	1.6 BSC	0.4 BSC	0.015	0.05	0.06
	nom			0.405	0.228	1.965		1.965					
	min		0.139	0.385	0.208	1.940		1.940					

wlcsp25_sot8117_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP25_SOT8117						25-05-12

Fig. 26. Package outline WLCSP25_SOT8117 (WLCSP25)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
AMOLED	Active-Matrix/Organic Light-Emitting Diode
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FD	Fast Discharge
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LED	Light-Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OLED	Organic Light-Emitting Diode
OTSD	Overtemperature Shutdown
PSM	Pulse Skip Mode
PWM	Pulse Width Modulation
SCP	Short-Circuit Protection
UVLO	Under-Voltage LockOut

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX10058 v.1.1	20251224	Product data sheet	-	NEX10058 v.1
Modifications:	• Overall update.			
NEX10058 v.1	20251113	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 24 December 2025