



GAN039-650NTB

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212i package

22 October 2025

Product data sheet

1. General description

The GAN039-650NTB is a 650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212i inverted package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Simplified driver design as standard level MOSFET gate drivers can be used:
 - 0 V to 12 V drive voltage
 - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ± 20 V V_{GS} rating
- High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
 - Improved reliability, with reduced $R_{th(j-mb)}$ for optimal cooling
 - Lower inductances for lower switching losses and EMI
 - 150 °C maximum junction temperature
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$-55\text{ °C} \leq T_j \leq 150\text{ °C}$		-	-	650	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	58.5	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	250	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 32\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	33	39	mΩ

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212i package

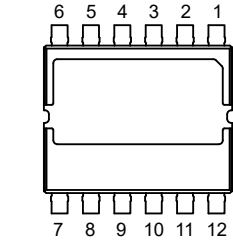
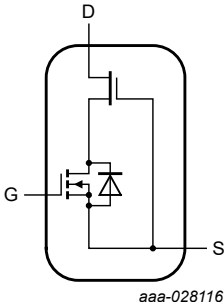
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}$; $I_D = 32\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$; Fig. 11		-	73	86	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 32\text{ A}$; $V_{DS} = 400\text{ V}$; $V_{GS} = 10\text{ V}$;		-	5	-	nC
$Q_{G(tot)}$	total gate charge	$T_j = 25\text{ }^{\circ}\text{C}$; Fig. 12 ; Fig. 13		-	26	-	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 32\text{ A}$; $di_S/dt = -1000\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; Fig. 19	[2]	-	187	-	nC

[1] The ID value is calculated based on the maximum thermal resistance from junction to mounting base and the RDSon

[2] $Q_r = Q_{oss} + Q_d$ where Q_d is charge associated with minority carriers in the body diode of the Si mosfet of the cascode.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 CCPAK1212i (SOT8005)	 aaa-028116
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN039-650NTB	CCPAK1212i	Plastic, surface mounted copper clip package inverted (CCPAK1212i); 13 terminals; 2.0 mm pitch, 12 mm x 9.4 mm x 2.5 mm body	SOT8005

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN039-650NTB	039INTB

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$-55\text{ }^{\circ}\text{C} \leq T_J \leq 150\text{ }^{\circ}\text{C}$		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; $t_p = 1\text{ }\mu\text{s}$; $\delta_{\text{factor}} = 0.01$		-	725	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{\text{mb}} = 25\text{ }^{\circ}\text{C}$; Fig. 1		-	250	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{\text{mb}} = 25\text{ }^{\circ}\text{C}$; Fig. 2	[1]	-	58.5	A
		$V_{GS} = 10\text{ V}$; $T_{\text{mb}} = 100\text{ }^{\circ}\text{C}$; Fig. 2		-	37	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ }^{\circ}\text{C}$; Fig. 3		-	234	A
T_{stg}	storage temperature			-55	150	$^{\circ}\text{C}$
T_J	junction temperature			-55	150	$^{\circ}\text{C}$
$T_{\text{sld(M)}}$	peak soldering temperature			-	260	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{\text{mb}} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 0\text{ V}$		-	58.5	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ }^{\circ}\text{C}$		-	234	A

[1] The I_D value is calculated based on the maximum thermal resistance from junction to mounting base and the R_{DSon}

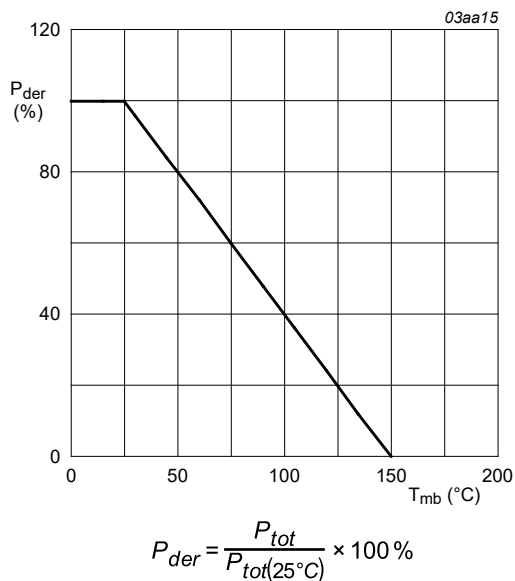
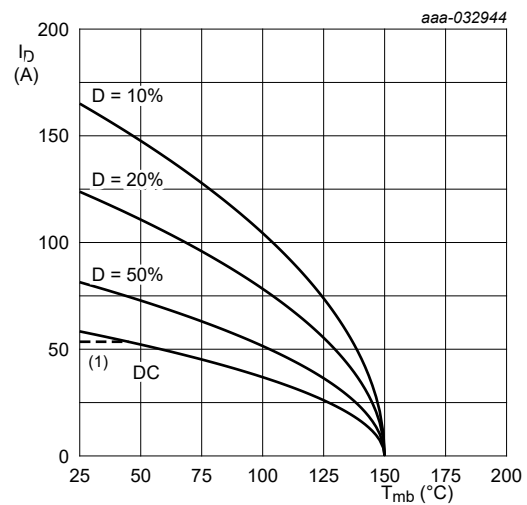


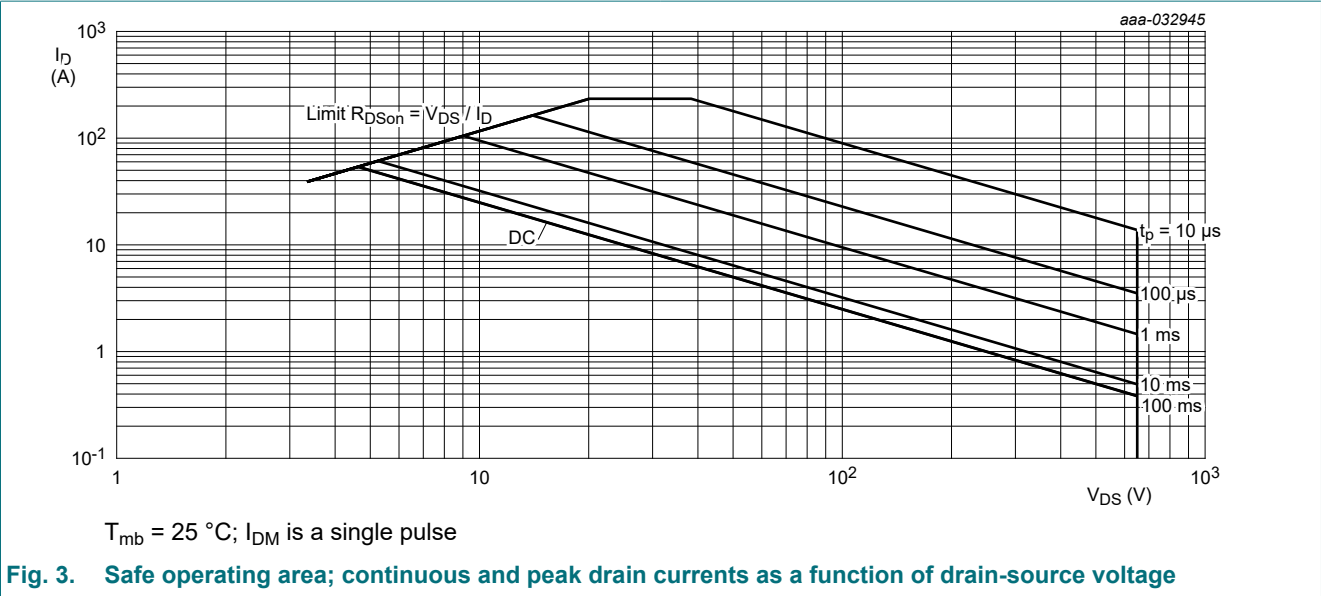
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

(1) 53.5A DC continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

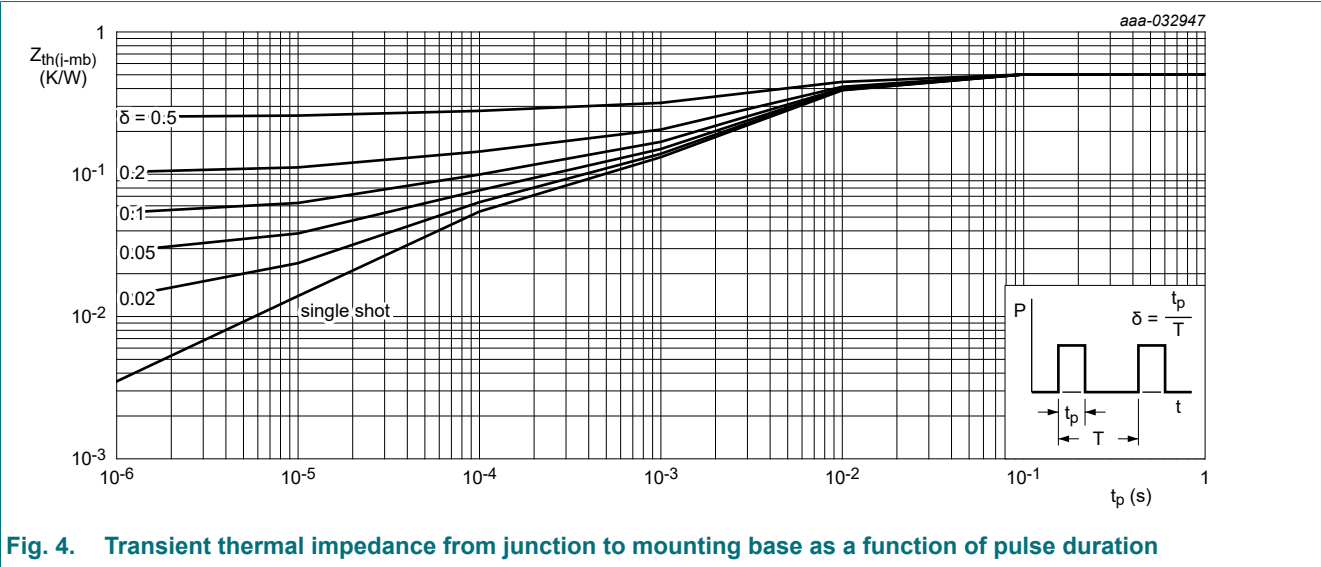
Fig. 2. Continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	0.5	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 25\text{ °C}$		3.4	3.9	4.6	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 150\text{ °C}$; Fig. 9		2.4	-	-	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = -55\text{ °C}$; Fig. 9		-	-	5.2	V
I_{DSS}	drain leakage current	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$		-	2.5	20	μA
		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 150\text{ °C}$		-	6	-	μA
I_{GSS}	gate leakage current	$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ °C}$		-	10	400	nA
		$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ °C}$		-	10	400	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 32\text{ A}$; $T_J = 25\text{ °C}$; Fig. 10		-	33	39	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 32\text{ A}$; $T_J = 150\text{ °C}$; Fig. 11		-	73	86	m Ω
R_G	gate resistance	$f = 1\text{ MHz}$		0.2	0.5	1.3	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 32\text{ A}$; $V_{DS} = 400\text{ V}$; $V_{GS} = 10\text{ V}$; $T_J = 25\text{ °C}$; Fig. 12 ; Fig. 13		-	26	-	nC
Q_{GS}	gate-source charge			-	10.2	-	nC
Q_{GD}	gate-drain charge			-	5	-	nC
C_{iss}	input capacitance	$V_{DS} = 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ °C}$; Fig. 14		-	1980	-	pF
C_{oss}	output capacitance			-	144	-	pF
C_{rss}	reverse transfer capacitance			-	1.6	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ °C}$; Fig. 15		-	218	-	pF
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ °C}$		-	432	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400\text{ V}$; $R_L = 12.5\text{ }\Omega$; $V_{GS} = 12\text{ V}$; $R_{G(ext)} = 12\text{ }\Omega$; Fig. 16 ; Fig. 17		-	17	-	ns
t_r	rise time			-	10	-	ns
$t_{d(off)}$	turn-off delay time			-	28	-	ns
t_f	fall time			-	9	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$		-	173	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 32\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$; Fig. 18		-	1.6	-	V
		$I_S = 16\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$; Fig. 18		-	1.2	-	V
t_{rr}	reverse recovery time	$I_S = 32\text{ A}$; $dI_S/dt = -1000\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; Fig. 19		-	25	-	ns
Q_r	recovered charge		[1]	-	187	-	nC

[1] $Q_r = Q_{oss} + Q_d$ where Q_d is charge associated with minority carriers in the body diode of the Si mosfet of the cascode.

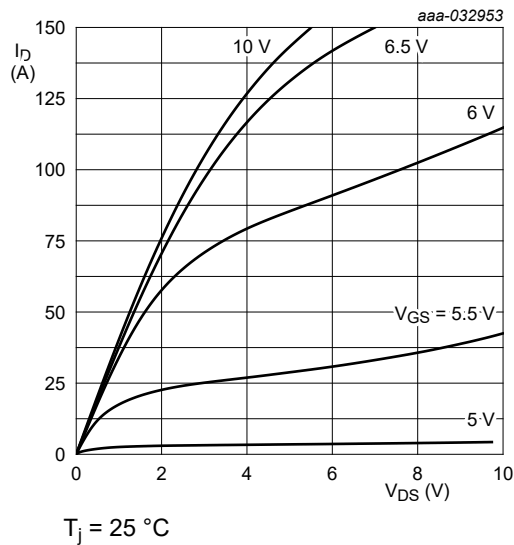


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

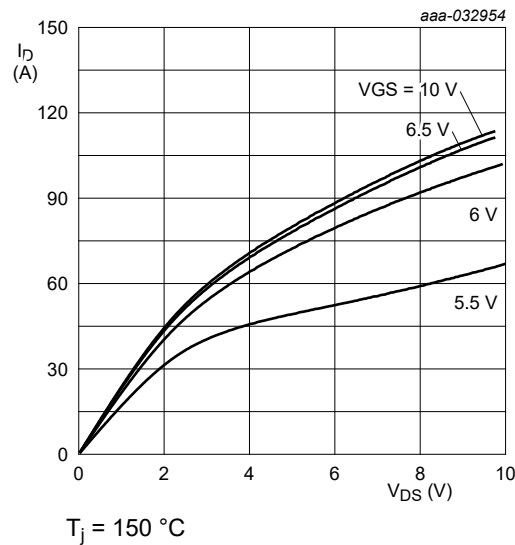


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

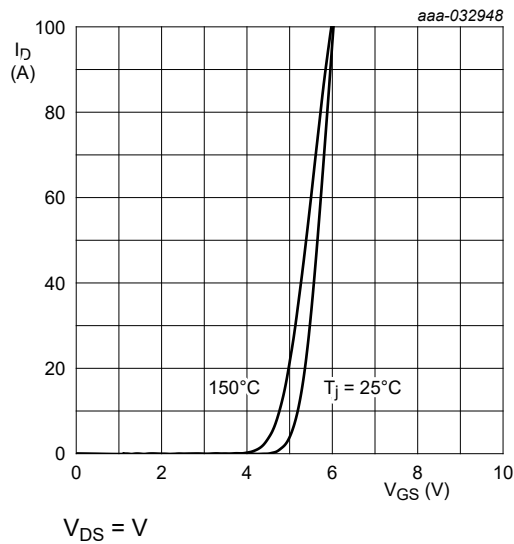


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

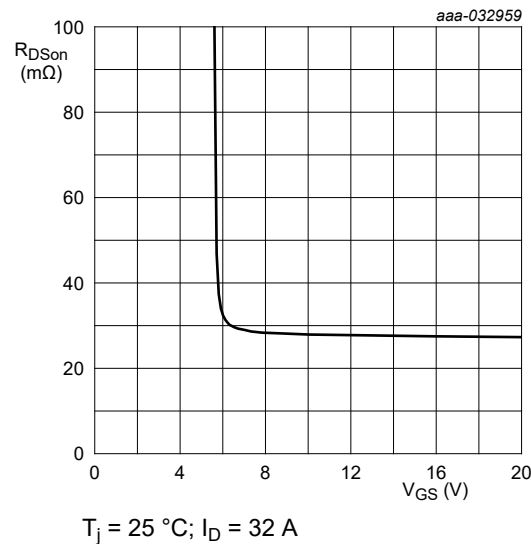
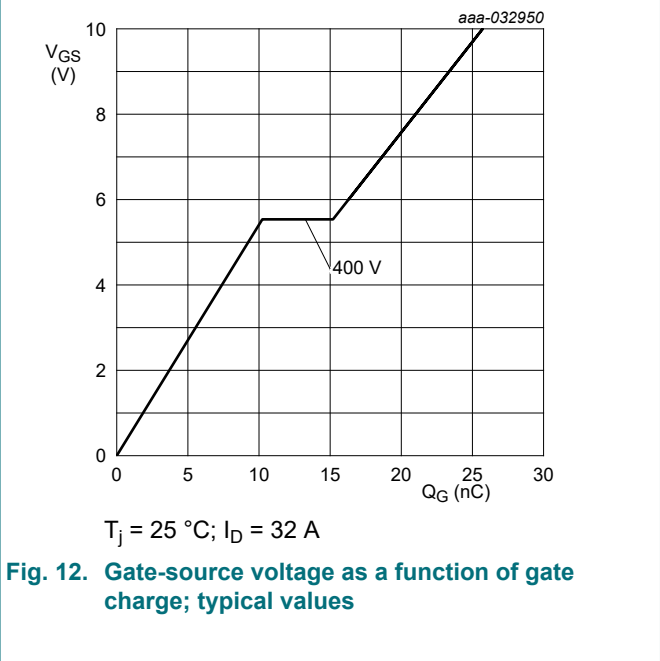
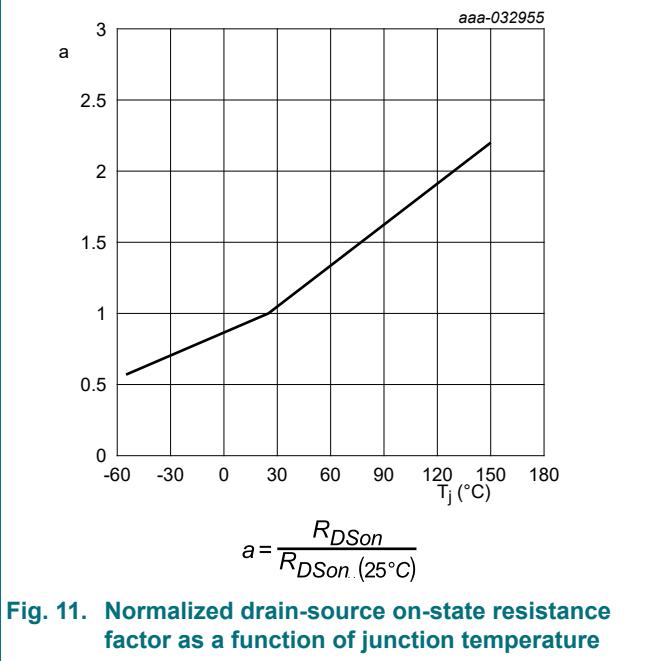
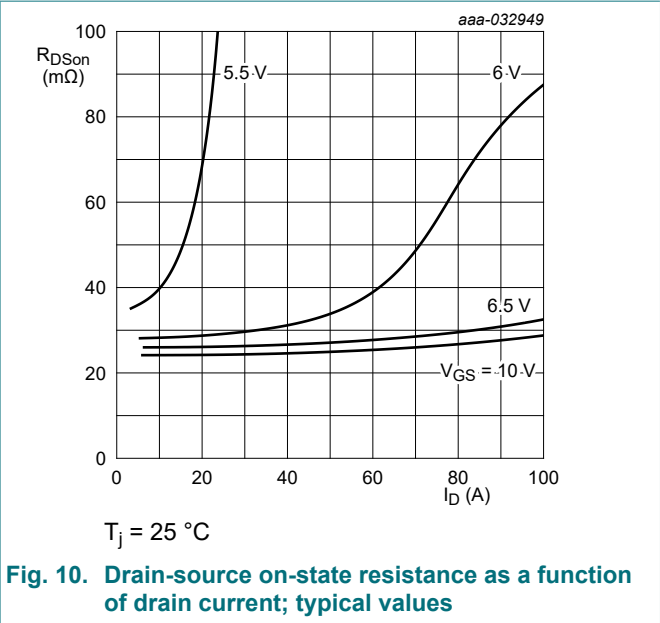
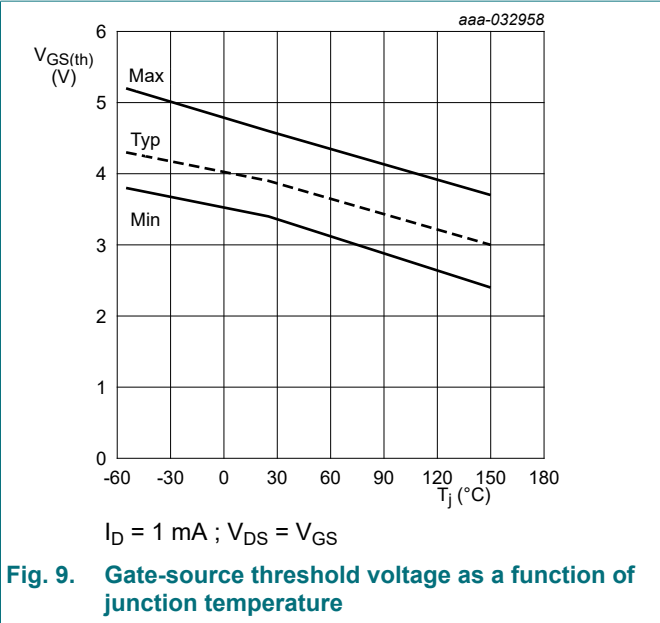


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



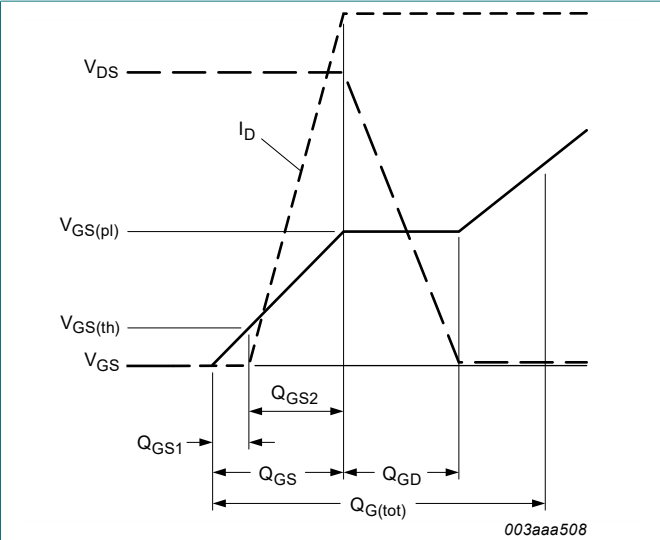


Fig. 13. Gate charge waveform definitions

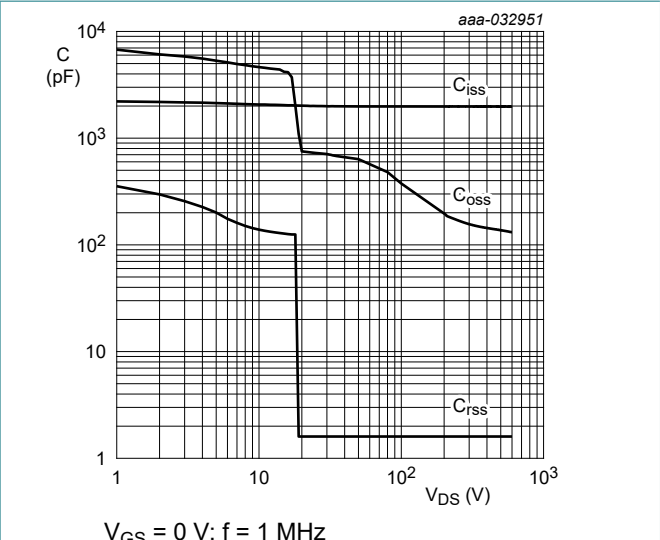


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

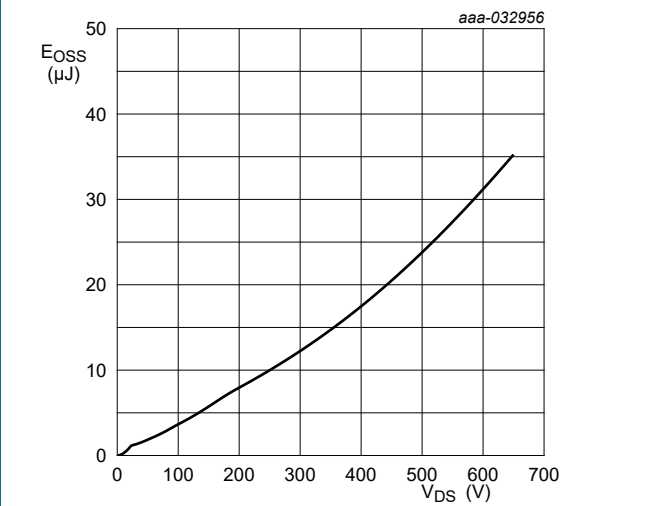


Fig. 15. Typical COSS Stored Energy

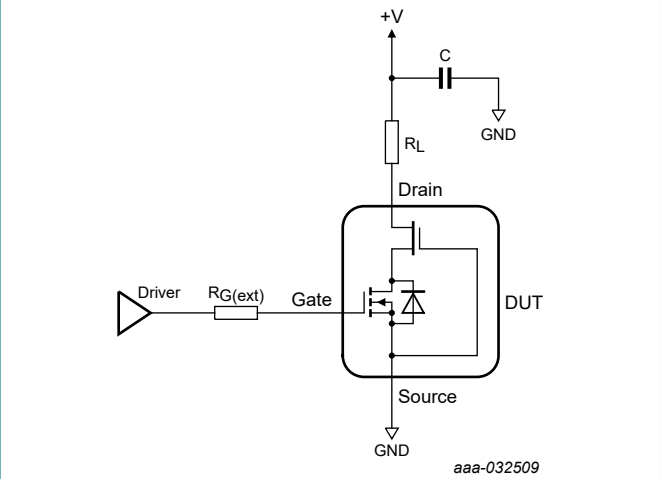


Fig. 16. Switching time test circuit

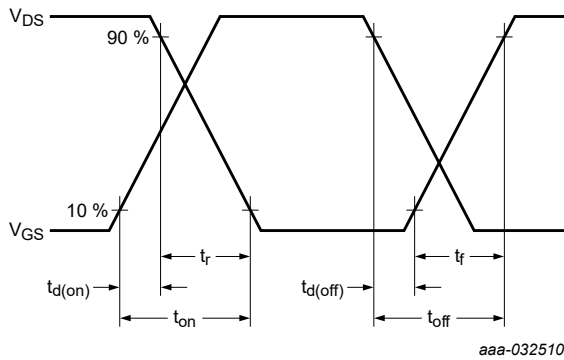


Fig. 17. Switching time waveform

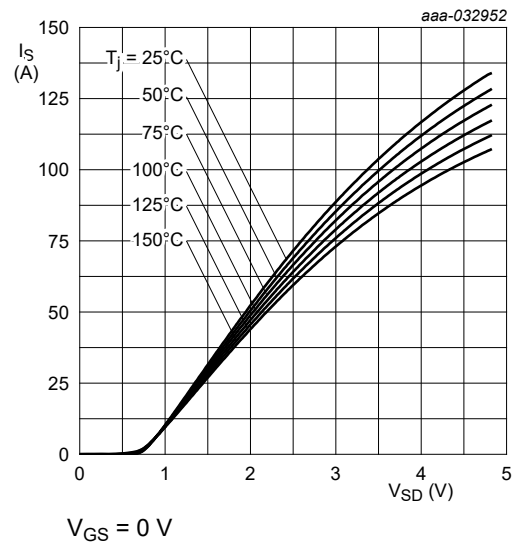


Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

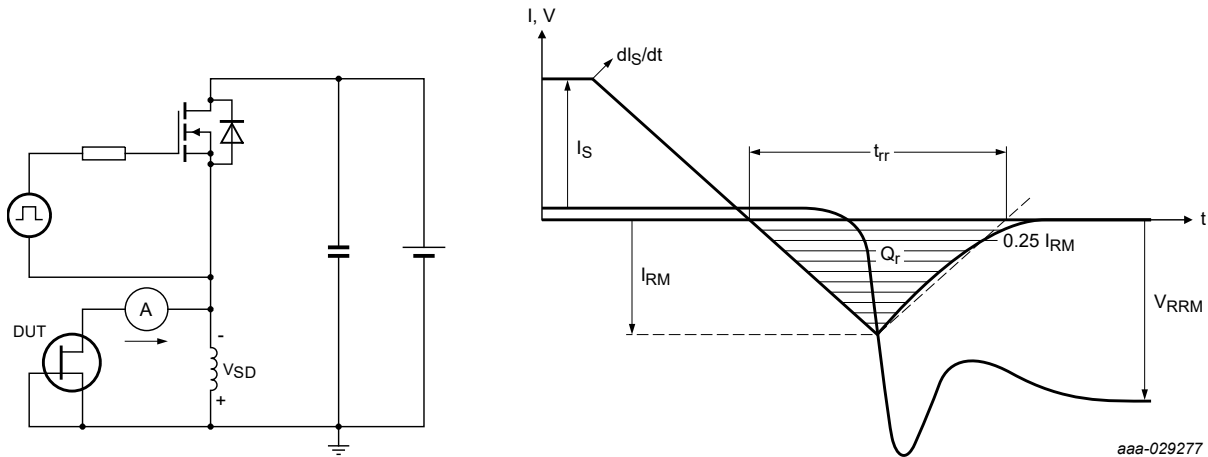


Fig. 19. Diode reverse recovery test circuit and waveform

11. Application information

A Ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin, (see figure below). Keeping the gate-source loop as compact as possible minimizes the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be $30 \, \Omega$ @ 100 MHz, (recommended p/n BLM18PG300SN1D). A series resistance (R_G) of 10 - 15 Ω is also recommended.

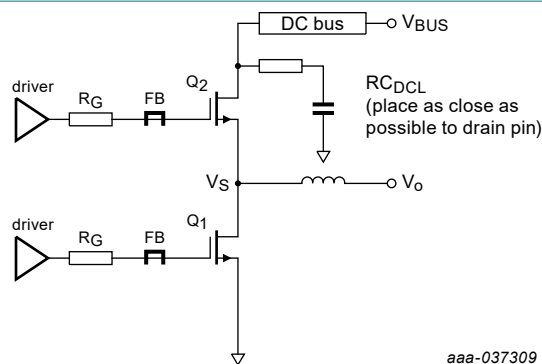


Fig. 20. Ferrite bead and RC resonance damper

A DC-link resonance damper is recommended in all cases. Optimal is 20 nF in series with 4 Ω , most easily achieved with parallel combination 10 nF and 8 Ω . This resonance damper lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability.

12. Package outline

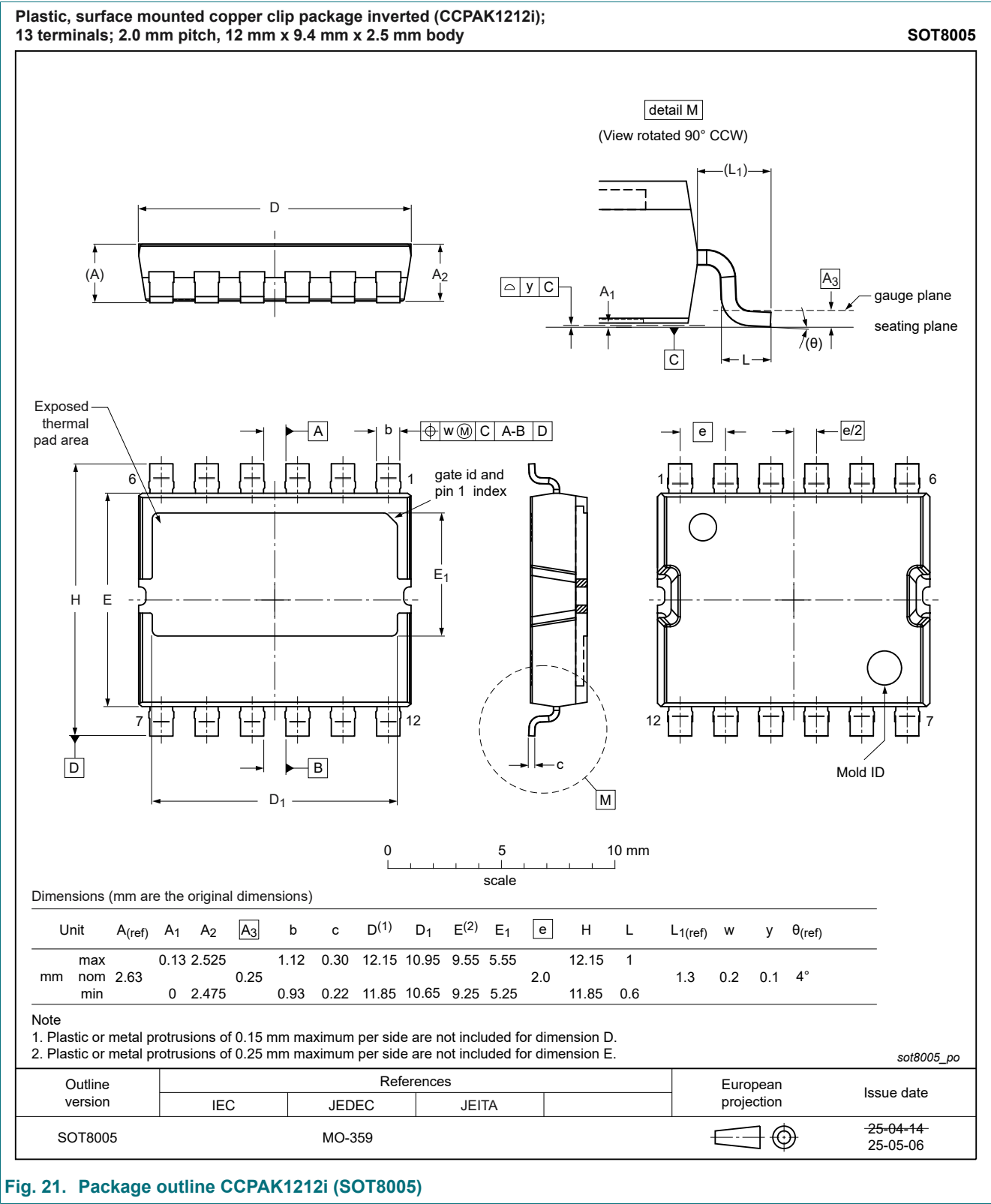


Fig. 21. Package outline CCPAK1212i (SOT8005)

13. Soldering

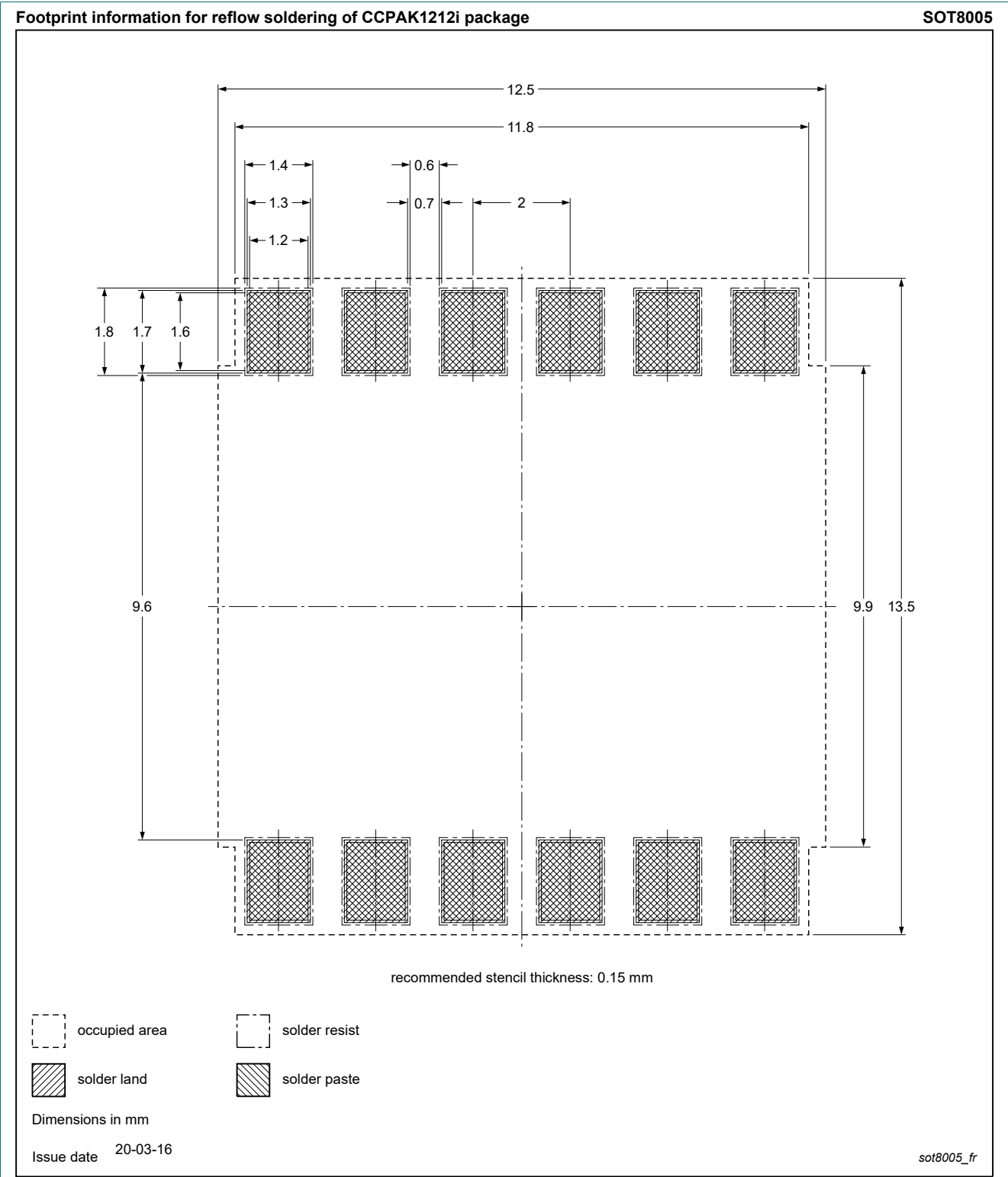


Fig. 22. Reflow soldering footprint for CCPAK1212i (SOT8005)

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 22 October 2025