



BUKNS1R0-40MYX8

40 V, 1.05 mΩ, Standard Level N-channel MOSFET in
MLPAK56-WF

Rev. 1 — 28 July 2026

Product data sheet

1. General Description

BUKNS1R0-40MYX8 is an automotive N-channel MOSFET using T2-40 low-ohmic split-gate technology, housed in an MLPAK56 (SOT8038) package. The MOSFET is qualified to AEC-Q101.

2. Features and Benefits

AEC-Q101 automotive qualification:

175 °C rating suitable for thermally demanding automotive environments

T2-40 split-gate trench technology:

Reduced cell-pitch enables enhanced power density resulting in lower conduction losses in same footprint

MLPAK micro-leads with side-wettable flanks:

Proven board-level reliability during thermal cycling

Visual (AOI) soldering inspection, no need for expensive X-ray equipment

Easy solder wetting for good mechanical solder joint

MLPAK copper-clip technology:

Improved reliability with reduced R_{th} , $R_{DS(on)}$, and package inductance

Increases maximum current capability and improves current spreading

3. Applications

- High reliability automotive systems
- Motor, lighting, and solenoid control
- Ultra high-performance power switching

4. Quick Reference Data

Table 1. Quick Reference Data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 [1]	-	-	220	A
Static Characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	0.5	0.89	1.05	mΩ
Dynamic Characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	77	92	nC

[1] Application tests show a continuous current of 220 A. The PCB, the thermal design, and the operating temperature limit the actual current.

5. Pinning Information

Table 2. Pinning Information

Pin	Symbol	Description	Simplified Outline	Graphic Symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering Information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUKNS1R0-40MYX8	MLPAK56	Plastic, thermal enhanced surface mounted package with side-wettable flanks (SWF); minileads; 8 terminals; pitch 1.27 mm; 5.6 x 5.15 x 1.0 mm body	SOT8038-4

7. Marking

Table 4. Marking Codes

Type Number	Marking Code
BUKNS1R0-40MYX8	BN1S004 X8MY

8. Limiting Values

Table 5. Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1	-	357	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2 [1]	-	220	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 2	-	220	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 3 [1]	-	1032	A
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$
Source-drain Diode					
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	220	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$	-	1032	A

Symbol	Parameter	Conditions	Min	Max	Unit
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 66\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 4 [2]	-	215	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4 [3]	-	220	A

- [1] Application tests show a continuous current of 220 A. The PCB, the thermal design, and the operating temperature limit the actual current.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
Refer to AN10273 for further information.
- [3] Protected by 100% test.

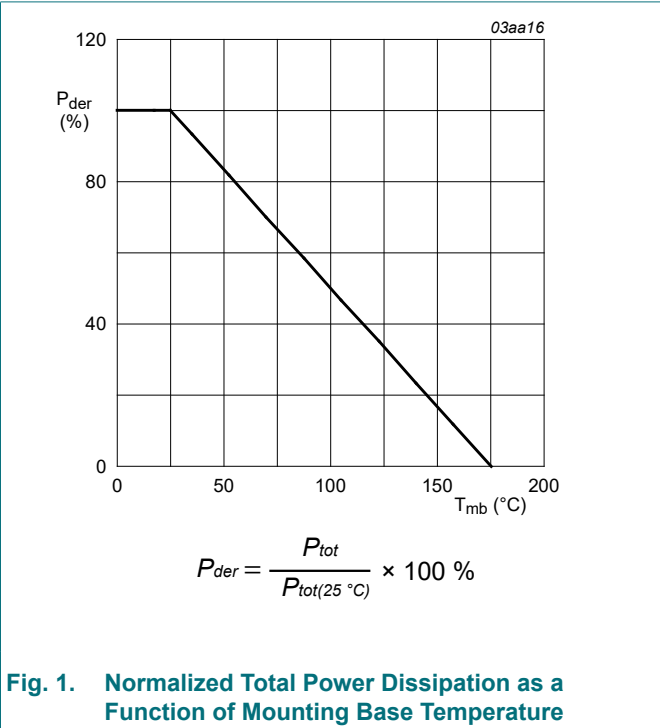


Fig. 1. Normalized Total Power Dissipation as a Function of Mounting Base Temperature

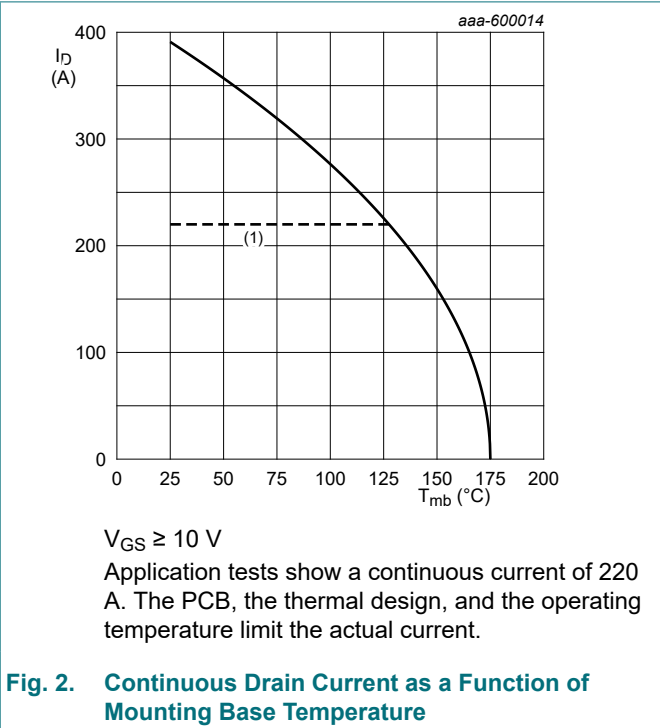


Fig. 2. Continuous Drain Current as a Function of Mounting Base Temperature

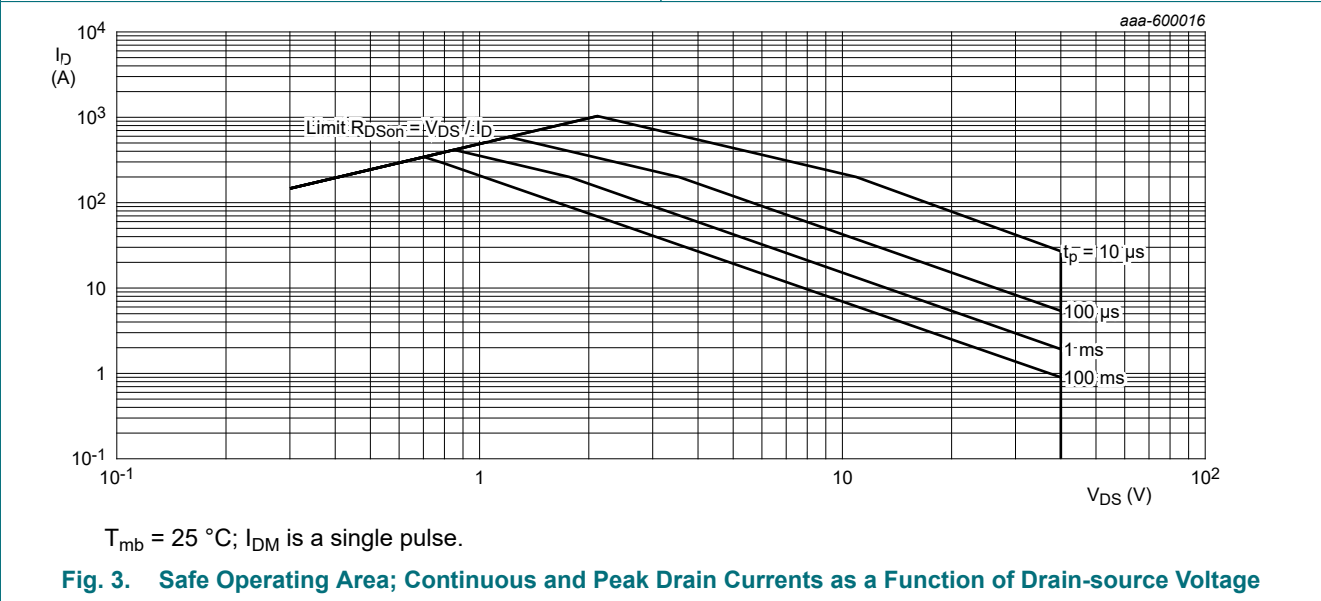
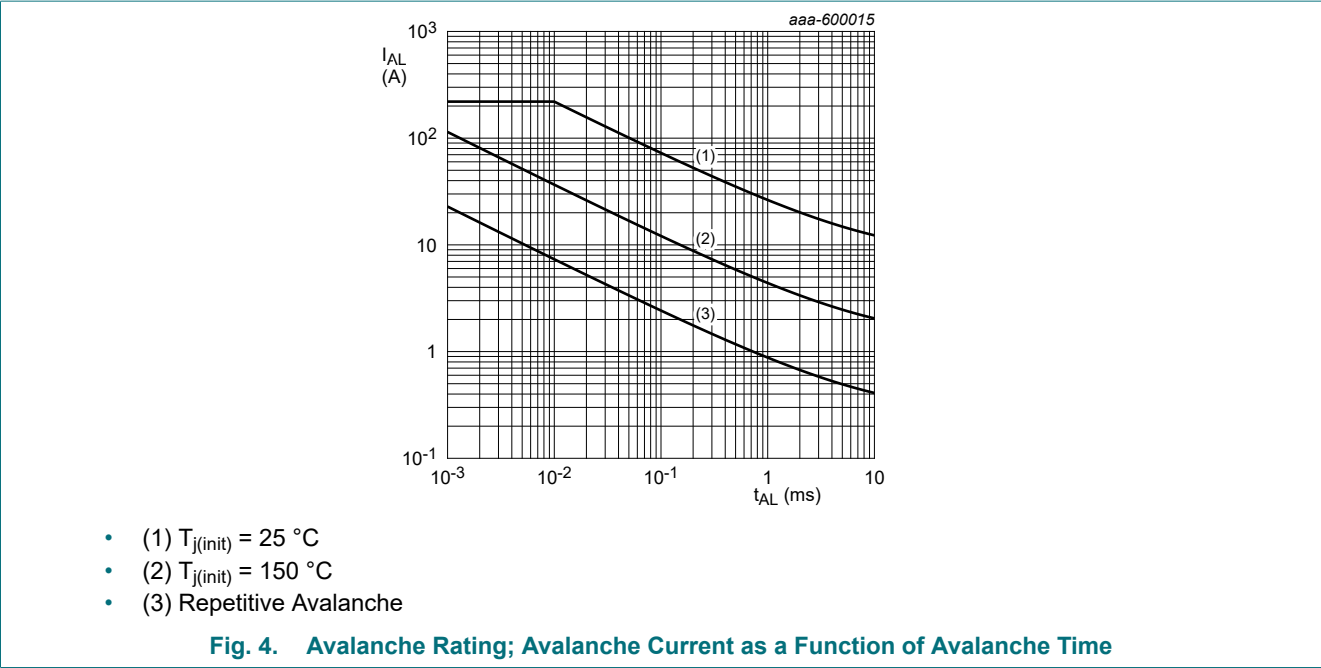


Fig. 3. Safe Operating Area; Continuous and Peak Drain Currents as a Function of Drain-source Voltage

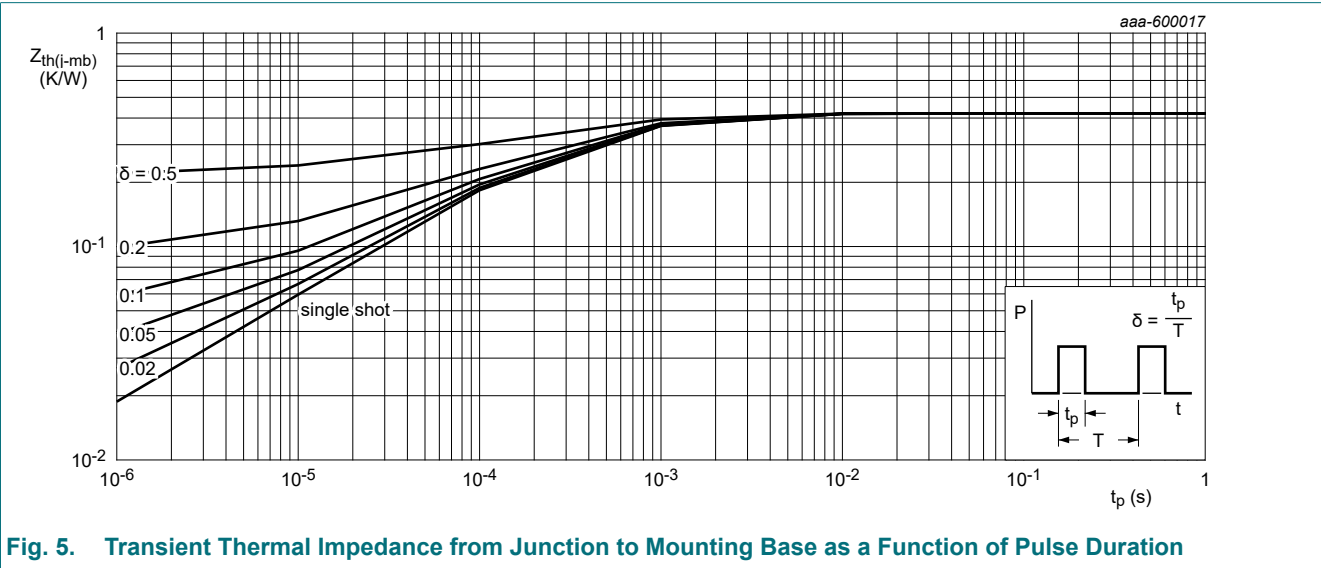


9. Thermal Characteristics

Table 6. Thermal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.32	0.42	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient ^[1]		-	24	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	40	44	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -40 °C	-	43.4	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	36	41.8	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 0.45 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10	2.3	3	3.7	V
		I _D = 0.45 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10	-	-	4.1	V
		I _D = 0.45 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.08	1	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _j = 125 °C	-	3	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	110	200	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	20	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	0.89	1.05	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 12	1.04	1.3	1.58	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 12	1.12	1.4	1.73	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12	1.36	1.7	2.1	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	0.16	0.56	1.12	Ω
Dynamic Characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13 ; Fig. 14	-	77	92	nC
Q _{GS}	gate-source charge		-	23	33	nC
Q _{GD}	gate-drain charge		-	16	24	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15	-	5373	8060	pF
C _{oss}	output capacitance		-	1366	2049	pF
C _{rss}	reverse transfer capacitance		-	16	24	pF
t _{d(on)}	turn-on delay time	V _{DS} = 32 V; R _L = 1.3 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C	-	26.5	-	ns
t _r	rise time		-	17.6	-	ns
t _{d(off)}	turn-off delay time		-	56.2	-	ns
t _f	fall time		-	17.8	-	ns
Source-drain Diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16	-	0.8	1	V
t _{rr}	reverse recovery time	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 17 [1]	-	59	-	ns
Q _r	recovered charge		-	83	-	nC

[1] Includes capacitive recovery

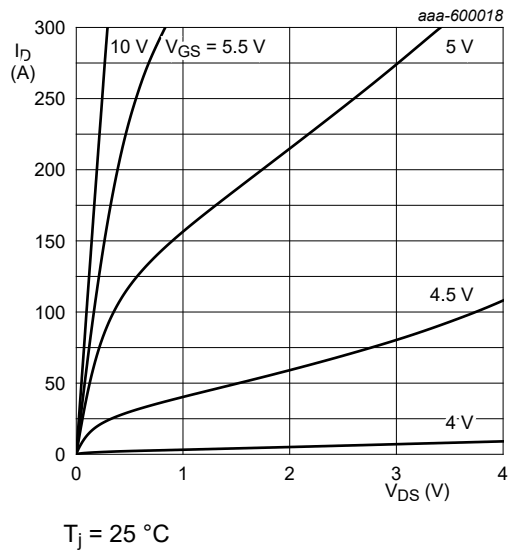


Fig. 6. Output Characteristics; Drain Current as a Function of Drain-source Voltage; Typical Values

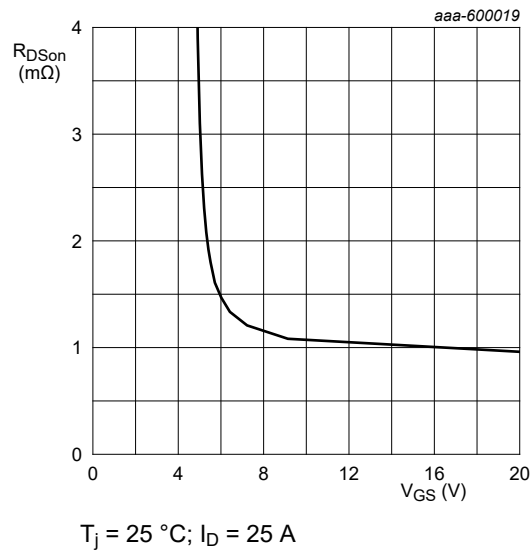


Fig. 7. Drain-source On-state Resistance as a Function of Gate-source Voltage; Typical Values

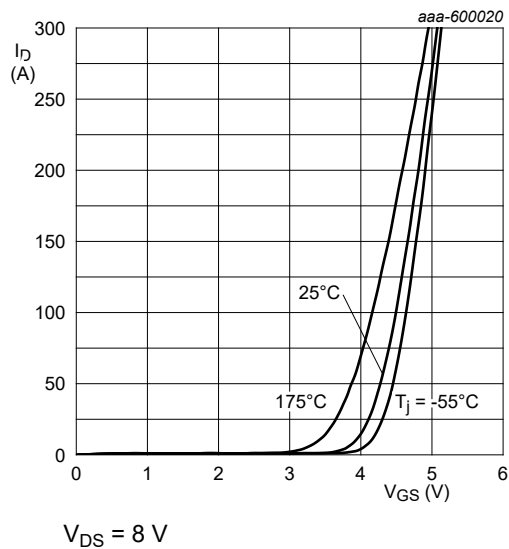


Fig. 8. Transfer Characteristics; Drain Current as a Function of Gate-source Voltage; Typical Values

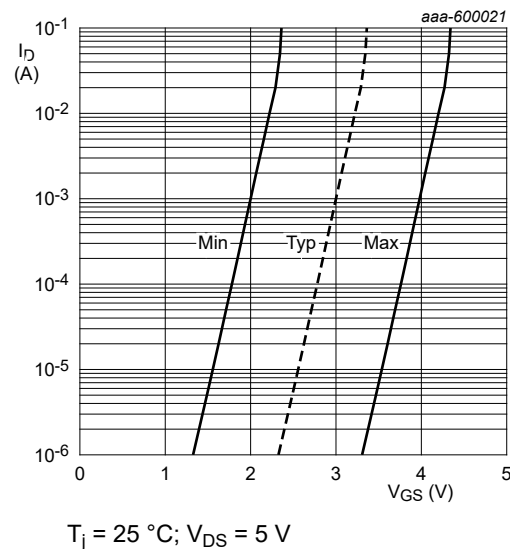
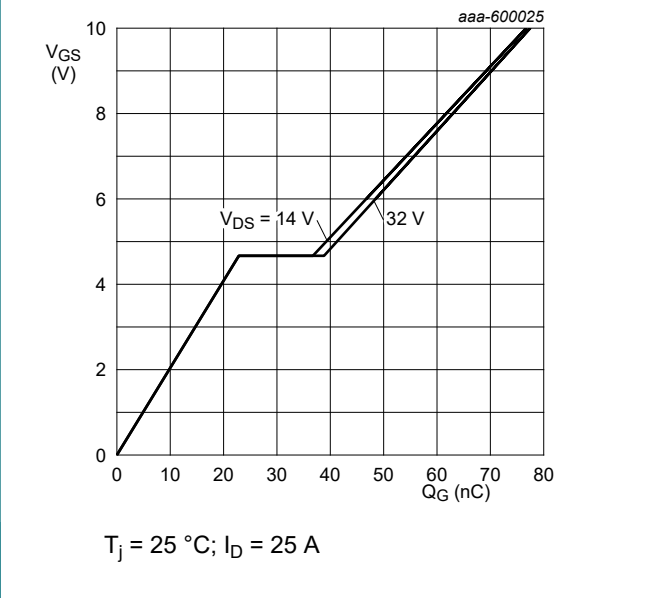
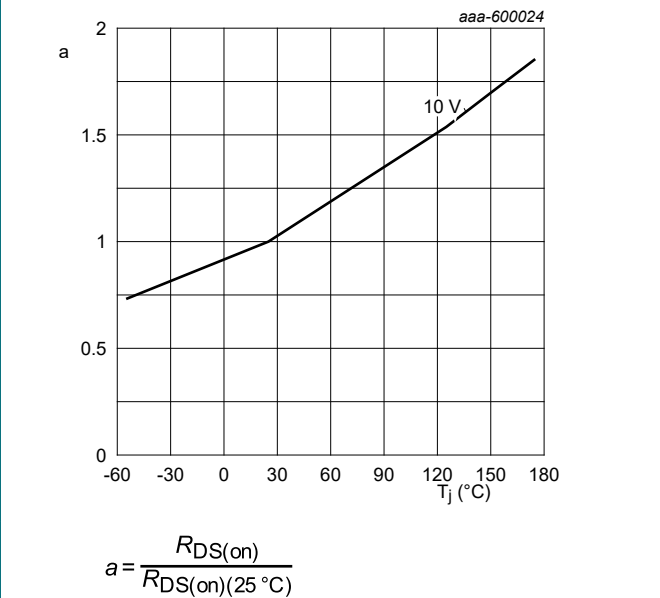
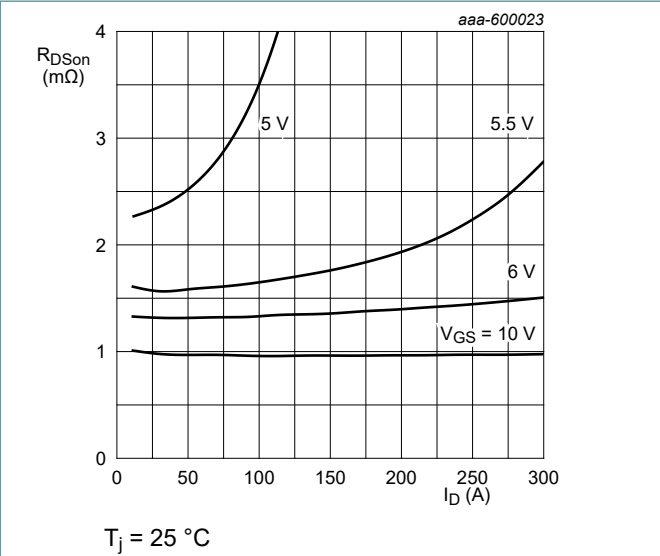
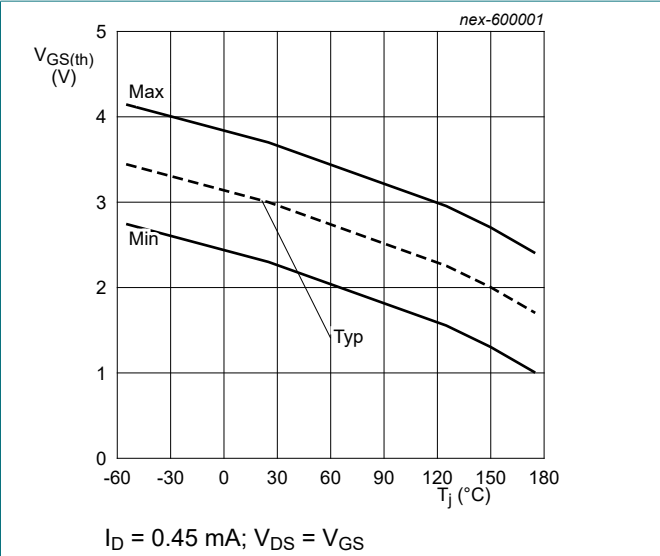


Fig. 9. Sub-threshold Drain Current as a Function of Gate-source Voltage



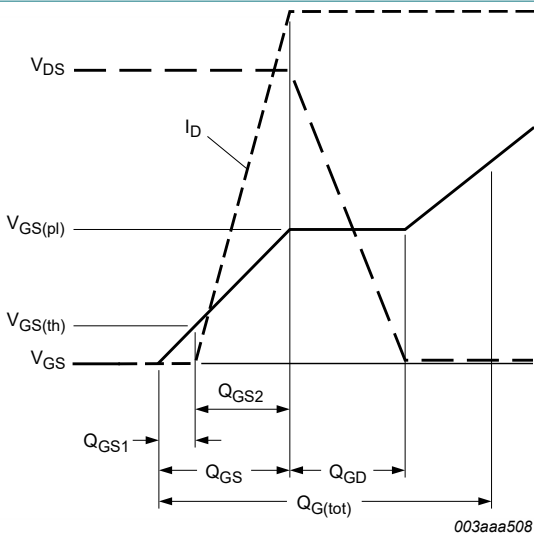
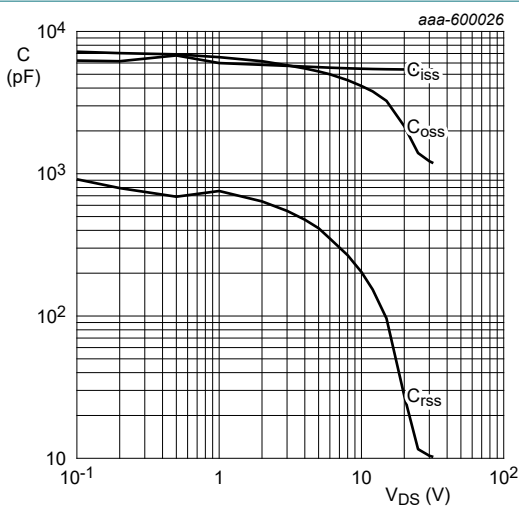
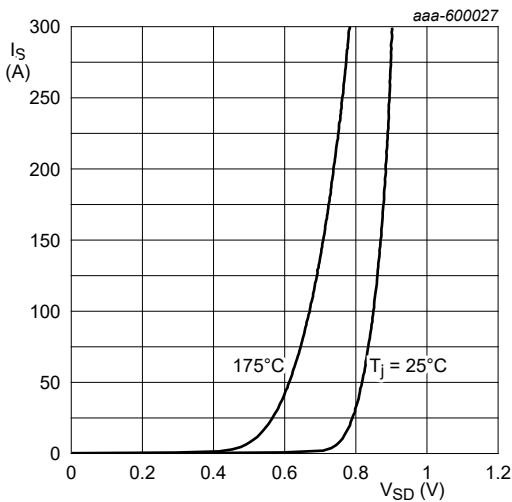


Fig. 14. Gate Charge Waveform Definitions



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 15. Input, Output, and Reverse Transfer Capacitances as a Function of Drain-source Voltage; Typical Values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (Diode Forward) Current as a Function of Source-drain (Diode Forward) Voltage; Typical Values

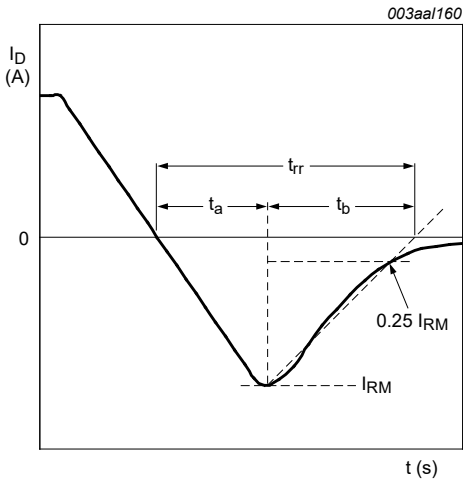


Fig. 17. Reverse Recovery Timing Definition

11. Package Outline

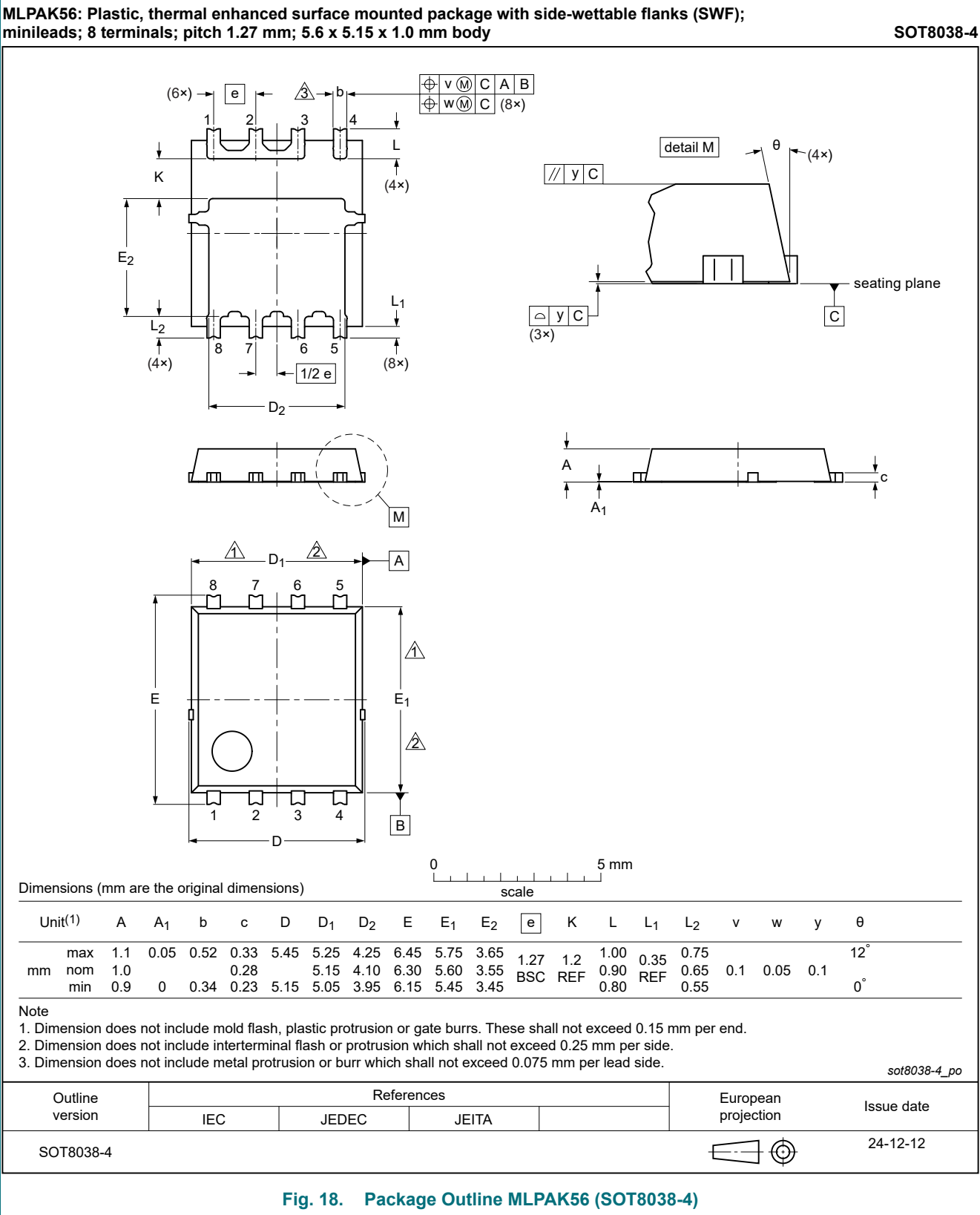


Fig. 18. Package Outline MLPAK56 (SOT8038-4)

12. Soldering

Table 8. Soldering

The diagram illustrates the reflow soldering footprint for the MLPAK56 (SOT8038-4) package. It shows a top-down view of the package with various dimensions and a legend.

Dimensions (mm):

- Overall width: 5.7
- Overall height: 7.4
- Width of central area: 4.51
- Width of central area (excluding leads): 4.41
- Lead width: 0.25 (2x)
- Lead spacing: 1.2 (6x)
- Lead height: 0.25 (2x)
- Lead spacing (bottom): 1.3 (6x)
- Lead height (bottom): 0.925
- Lead width (bottom): 1.15
- Lead width (bottom): 1.3 (8x)
- Lead width (bottom): 1.35 (4x)
- Lead width (bottom): 1.45 (4x)
- Lead width (bottom): 0.7 (8x)
- Lead width (bottom): 0.6 (8x)
- Lead width (bottom): 0.55 (8x)
- Lead width (bottom): 1.27
- Lead width (bottom): 0.45
- Lead width (bottom): 1.05
- Lead width (bottom): 1.1
- Lead width (bottom): 2.45
- Lead width (bottom): 2.5
- Lead width (bottom): 3.5
- Lead width (bottom): 3.55

Legend:

- occupied area (dashed line)
- solder resist (dashed line)
- solder land (solid line)
- solder paste (solid line)

recommended stencil thickness: 0.125 mm

Fig. 19. Reflow Soldering Footprint for MLPAK56 (SOT8038-4)

13. Revision History

Table 9. Revision History

Document ID	Release Date	Data Sheet Status	Supersedes
BUKNS1R0-40MYX8 v. 1	20260728	Product data sheet	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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