74HCS596-Q100

8-bit shift register with Schmitt-trigger inputs and open-drain output registers

Rev. 1 — 28 May 2025 Product data sheet

1. General description

The 74HCS596-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- Schmitt-trigger inputs
- Low power consumption
  - Typical supply current (I_{CC}) of 100 nA
  - Typical input leakage current (I_I) of ±10 nA
- ±7.8 mA output drive at 6 V
- 8-bit serial input and 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
  - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Multiple package options

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register
- Output expansion
- LED matrix control
- 7-segment display control

- 8-bit data storage

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCS596D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCS596PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCS596BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

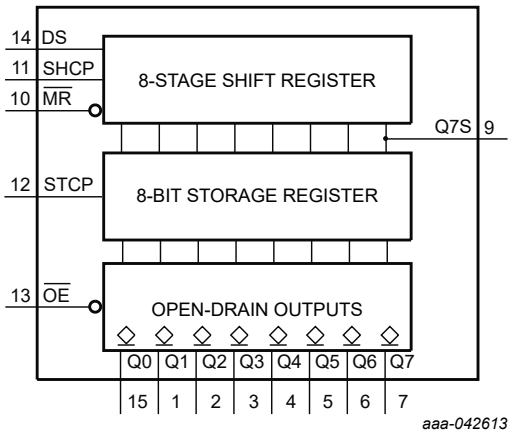


Fig. 1. Functional diagram

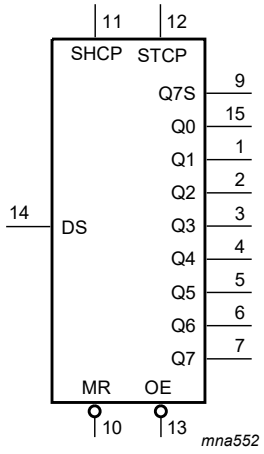


Fig. 2. Logic symbol

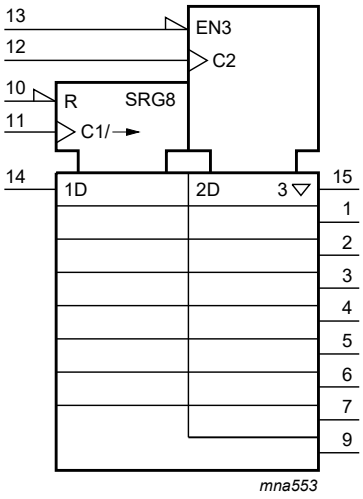


Fig. 3. IEC logic symbol

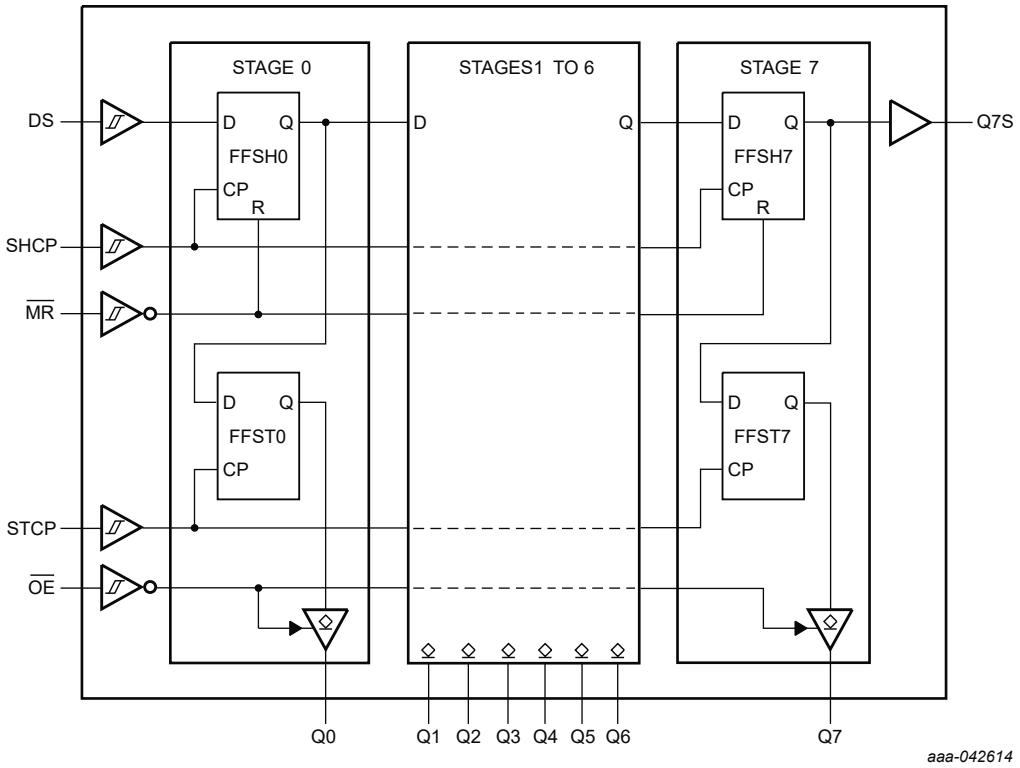
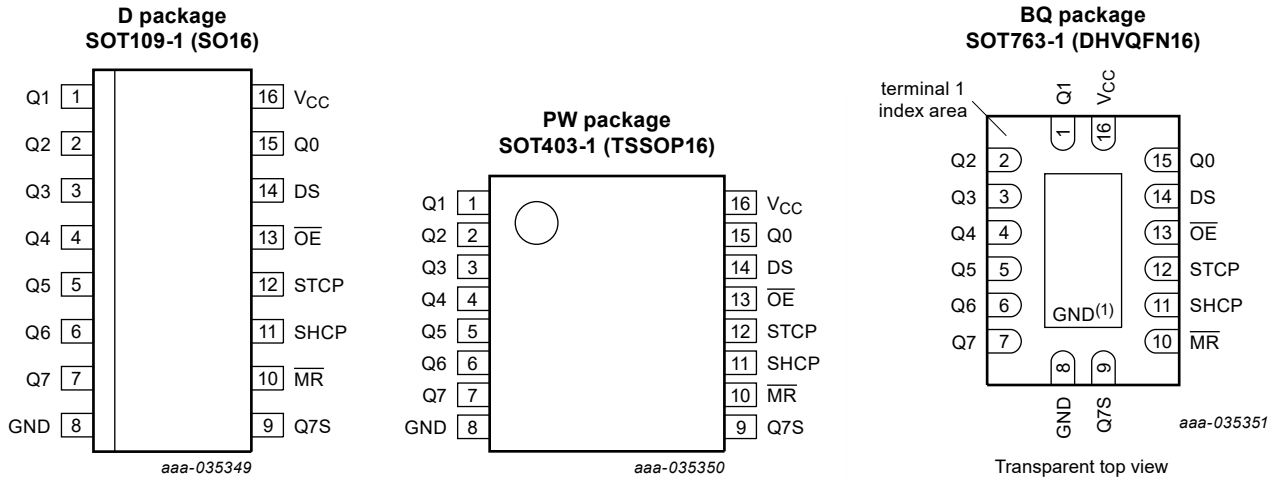


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data outputs (open-drain)
GND	8	ground (0 V)
Q7S	9	serial data output, can be used for cascading
$\overline{MR}$	10	master reset, clears shift register (active LOW)
SHCP	11	shift register clock, rising edge triggered
STCP	12	storage register clock, rising edge triggered
$\overline{OE}$	13	output enable (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition;
X = don't care; NC = no change; Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

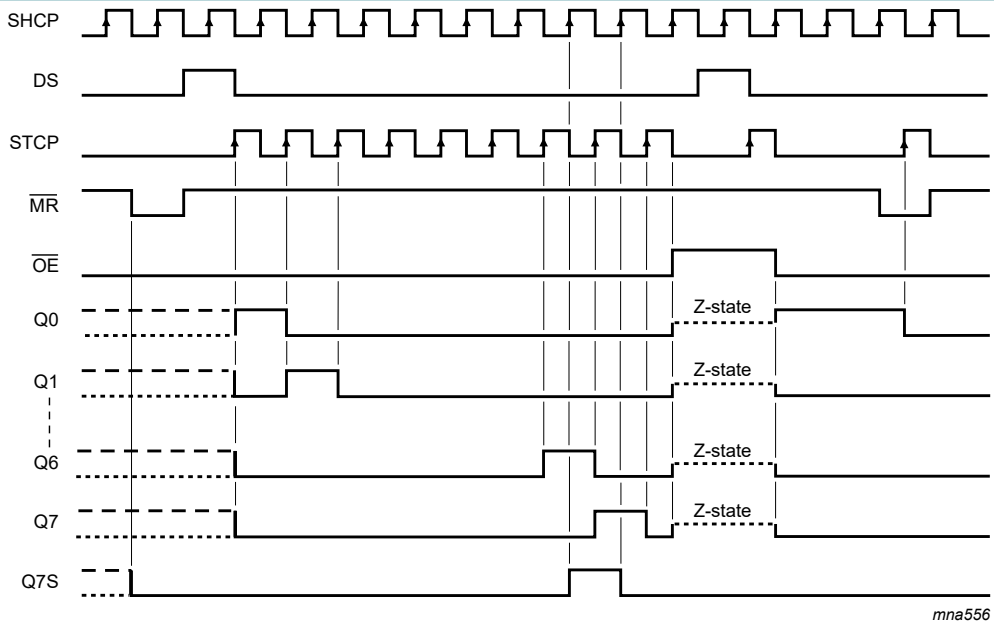


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_j	junction temperature	[2]	-	+150	°C
T_{stg}	storage temperature		-65	+150	°C
V_{ESD}	electrostatic discharge	HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4000 V	-	±4000	V
		CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1500 V	-	±1500	V
P_{tot}	total power dissipation	[3]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Guaranteed by design.
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 6 and Fig. 7								
		V_{CC} = 2.0 V	0.7	-	1.5	0.7	1.5	0.7	1.5	V
		V_{CC} = 4.5 V	1.7	-	3.15	1.7	3.15	1.7	3.15	V
		V_{CC} = 6 V	2.1	-	4.2	2.1	4.2	2.1	4.2	V
		V_{CC} = 3.0 V to 3.6 V	$0.4V_{CC}$	-	$0.7V_{CC}$	$0.4V_{CC}$	$0.7V_{CC}$	$0.4V_{CC}$	$0.7V_{CC}$	V
		V_{CC} = 4.5 V to 5.5 V	$0.38V_{CC}$	-	$0.7V_{CC}$	$0.38V_{CC}$	$0.7V_{CC}$	$0.38V_{CC}$	$0.7V_{CC}$	V
V_{T-}	negative-going threshold voltage	see Fig. 6 and Fig. 7								
		V_{CC} = 2.0 V	0.3	-	1.0	0.3	1.0	0.3	1.0	V
		V_{CC} = 4.5 V	0.9	-	2.2	0.9	2.2	0.9	2.2	V
		V_{CC} = 6 V	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		V_{CC} = 3.0 V to 3.6 V	$0.2V_{CC}$	-	$0.5V_{CC}$	$0.2V_{CC}$	$0.5V_{CC}$	$0.2V_{CC}$	$0.5V_{CC}$	V
		V_{CC} = 4.5 V to 5.5 V	$0.2V_{CC}$	-	$0.49V_{CC}$	$0.2V_{CC}$	$0.49V_{CC}$	$0.2V_{CC}$	$0.49V_{CC}$	V
V_H	hysteresis voltage[1]	see Fig. 6 and Fig. 7								
		V_{CC} = 2.0 V	0.2	0.52	1.0	0.2	1.0	0.2	1.0	V
		V_{CC} = 4.5 V	0.4	0.85	1.4	0.4	1.4	0.4	1.4	V
		V_{CC} = 6 V	0.6	1.1	1.6	0.6	1.6	0.6	1.6	V
		V_{CC} = 3.0 V to 3.6 V	$0.1V_{CC}$	0.72	$0.38V_{CC}$	$0.1V_{CC}$	$0.38V_{CC}$	$0.1V_{CC}$	$0.38V_{CC}$	V
		V_{CC} = 4.5 V to 5.5 V	$0.09V_{CC}$	0.94	$0.29V_{CC}$	$0.09V_{CC}$	$0.29V_{CC}$	$0.09V_{CC}$	$0.29V_{CC}$	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_{OH} = -20 µA; V_{CC} = 2.0 V to 6.0 V	V_{CC}-0.1	V_{CC}-0.002	-	V_{CC}-0.1	-	V_{CC}-0.1	-	V
		I_{OH} = -4 mA; V_{CC} = 3.0 V	2.7	2.85	-	2.7	-	2.7	-	V
		I_{OH} = -6 mA; V_{CC} = 4.5 V	4.0	4.3	-	4.0	-	4.0	-	V
		I_{OH} = -7.8 mA; V_{CC} = 6.0 V	5.48	5.75	-	5.4	-	5.4	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_{OL} = 20 µA; V_{CC} = 2.0 V to 6.0 V	-	0.002	0.1	-	0.1	-	0.1	V
		I_{OL} = 4 mA; V_{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I_{OL} = 6 mA; V_{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I_{OL} = 7.8 mA; V_{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	±0.01	±0.1	-	±0.25	-	±1.0	µA
I_{OZ}	OFF-state output current	V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	±0.05	±0.25	-	±1.0	-	±5.0	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	0.01	0.1	-	0.5	-	2.0	µA

[1] Guaranteed by design.

10.1. Transfer characteristic waveforms and graphs

10.1.1. For inputs

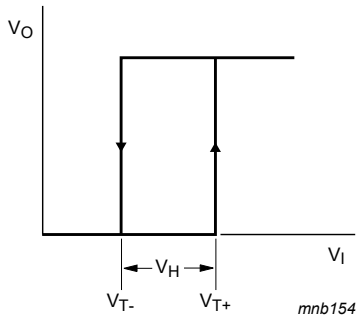


Fig. 6. Transfer characteristic

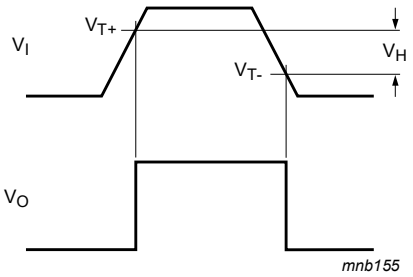
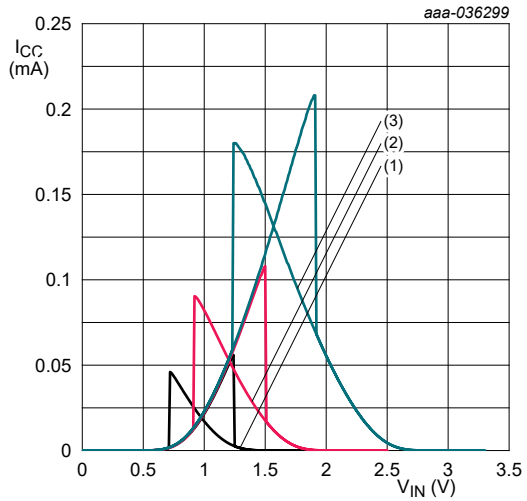
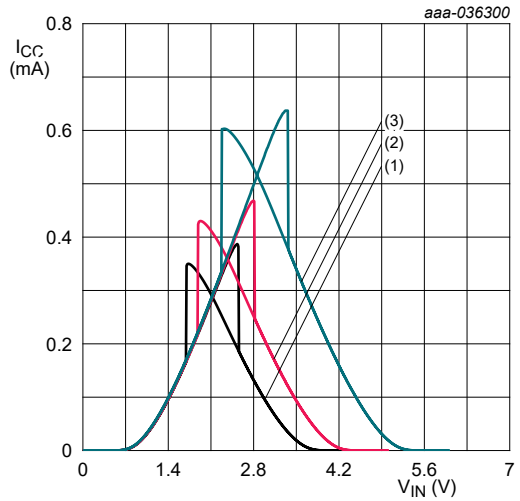


Fig. 7. Definitions of V_{T+}, V_{T-} and V_H



(1) V_{CC} = 2.0 V
(2) V_{CC} = 2.5 V
(3) V_{CC} = 3.3 V

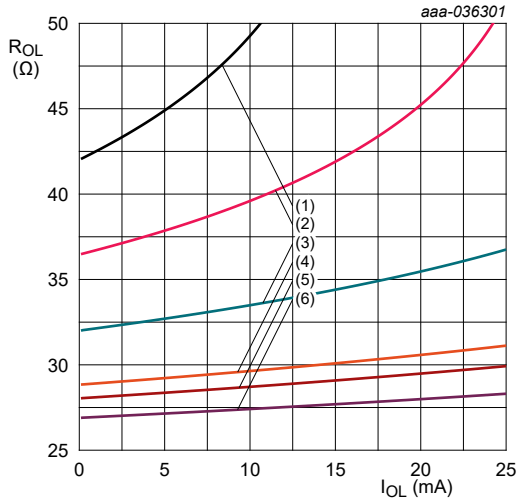
Fig. 8. Typical supply current vs the input voltage



(1) V_{CC} = 4.5 V
(2) V_{CC} = 5.0 V
(3) V_{CC} = 6.0 V

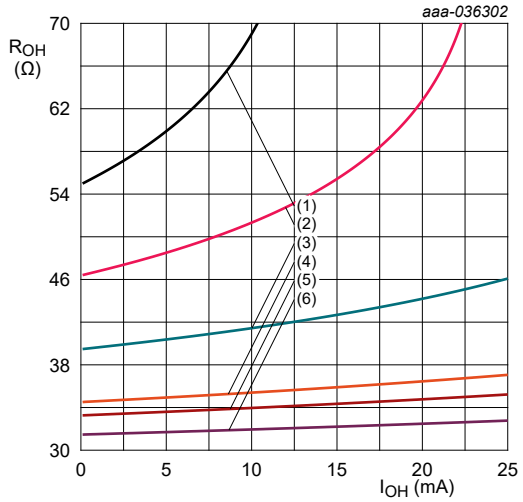
Fig. 9. Typical supply current vs the input voltage

10.1.2. For outputs



(1) V_{CC} = 2.0 V
(2) V_{CC} = 2.5 V
(3) V_{CC} = 3.3 V
(4) V_{CC} = 4.5 V
(5) V_{CC} = 5.0 V
(6) V_{CC} = 6.0 V

Fig. 10. Typical LOW-level output resistance as function of the output current



(1) V_{CC} = 2.0 V
(2) V_{CC} = 2.5 V
(3) V_{CC} = 3.3 V
(4) V_{CC} = 4.5 V
(5) V_{CC} = 5.0 V
(6) V_{CC} = 6.0 V

Fig. 11. Typical HIGH-level output resistance as function of the output current

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Section 11.1.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	SHCP to Q7S; see Fig. 12 [2]								
		V_{CC} = 2 V	-	14	19	-	40	-	45	ns
		V_{CC} = 4.5 V	-	6	8	-	22	-	25	ns
		V_{CC} = 6 V	-	5	7	-	19	-	21	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	8	-	22	-	25	ns
t_{PZL}	OFF-state to LOW propagation delay	STCP to Qn; see Fig. 13								
		V_{CC} = 2 V	-	16	21	-	40	-	45	ns
		V_{CC} = 4.5 V	-	6	9	-	22	-	25	ns
		V_{CC} = 6 V	-	6	8	-	19	-	21	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	9	-	22	-	25	ns

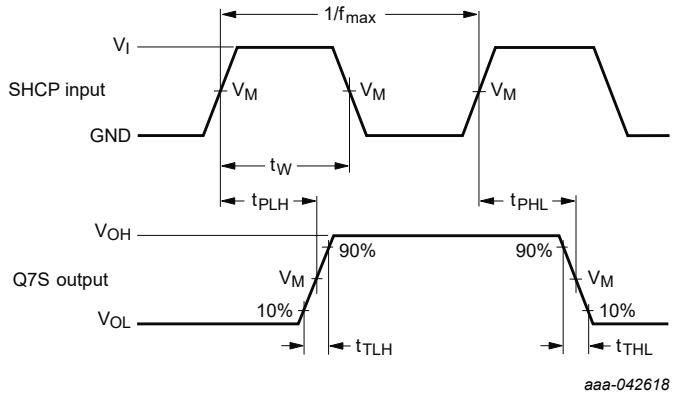
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{PLZ}	LOW to OFF-state propagation delay	STCP to Qn; see Fig. 13								
		V_{CC} = 2 V	-	11	16	-	40	-	45	ns
		V_{CC} = 4.5 V	-	8	11	-	22	-	25	ns
		V_{CC} = 6 V	-	7	10	-	19	-	21	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	11	-	22	-	25	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Q7S; see Fig. 15								
		V_{CC} = 2 V	-	13	19	-	40	-	45	ns
		V_{CC} = 4.5 V	-	6	8	-	22	-	25	ns
		V_{CC} = 6 V	-	6	8	-	19	-	21	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	8	-	22	-	25	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 16 [3]								
		V_{CC} = 2 V	-	12	18	-	25	-	27	ns
		V_{CC} = 4.5 V	-	6	9	-	11	-	13	ns
		V_{CC} = 6 V	-	5	8	-	10	-	11	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	9	-	11	-	13	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 16 [4]								
		V_{CC} = 2 V	-	13	16	-	19	-	20	ns
		V_{CC} = 4.5 V	-	9	11	-	12	-	13	ns
		V_{CC} = 6 V	-	8	10	-	11	-	12	ns
		V_{CC} = 3.0 V to 3.6 V	-	tbd	tbd	-	tbd	-	tbd	ns
		V_{CC} = 4.5 V to 5.5 V	-	tbd	11	-	12	-	13	ns
t_W	pulse width	SHCP, STCP, HIGH or LOW; see Fig. 12 and Fig. 13								
		V_{CC} = 2 V	7	-	-	8	-	9	-	ns
		V_{CC} = 4.5 V	7	-	-	7	-	7	-	ns
		V_{CC} = 6 V	7	-	-	7	-	7	-	ns
		V_{CC} = 3.0 V to 3.6 V	7	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	7	-	-	7	-	7	-	ns
		$\overline{MR}$ LOW; see Fig. 15								
		V_{CC} = 2 V	8	-	-	9	-	10	-	ns
		V_{CC} = 4.5 V	7	-	-	7	-	7	-	ns
		V_{CC} = 6 V	7	-	-	7	-	7	-	ns
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	7	-	-	7	-	7	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{su}	set-up time	DS to SHCP; see Fig. 14								
		V_{CC} = 2 V	8	-	-	11	-	13	-	ns
		V_{CC} = 4.5 V	4	-	-	5	-	5	-	ns
		V_{CC} = 6 V	3	-	-	4	-	4	-	ns
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	4	-	-	5	-	5	-	ns
		SHCP to STCP; see Fig. 13								
		V_{CC} = 2 V	11	-	-	16	-	18	-	ns
		V_{CC} = 4.5 V	5	-	-	6	-	7	-	ns
		V_{CC} = 6 V	4	-	-	5	-	6	-	ns
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	5	-	-	6	-	7	-	ns
		$\overline{MR}$ to SHCP; see Fig. 15								
		V_{CC} = 2 V	8	-	-	11	-	13	-	ns
		V_{CC} = 4.5 V	4	-	-	5	-	6	-	ns
		V_{CC} = 6 V	4	-	-	5	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	4	-	-	5	-	6	-	ns
t_h	hold time	DS to SHCP; see Fig. 14								
		V_{CC} = 2 V	0	-	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-	-	0	-	0	-	ns
		V_{CC} = 6 V	0	-	-	0	-	0	-	ns
		V_{CC} = 3.0 V to 3.6 V	0	-	-	0	-	0	-	ns
		V_{CC} = 4.5 V to 5.5 V	0	-	-	0	-	0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Fig. 15								
		V_{CC} = 2 V	8	-	-	10	-	13	-	ns
		V_{CC} = 4.5 V	4	-	-	5	-	6	-	ns
		V_{CC} = 6 V	4	-	-	5	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	ns
		V_{CC} = 4.5 V to 5.5 V	4	-	-	5	-	6	-	ns
f_{max}	maximum frequency	SHCP, STCP; see Fig. 12 and Fig. 13								
		V_{CC} = 2 V	35	-	-	21	-	19	-	MHz
		V_{CC} = 4.5 V	110	-	-	64	-	60	-	MHz
		V_{CC} = 6 V	130	-	-	78	-	75	-	MHz
		V_{CC} = 3.0 V to 3.6 V	tbd	-	-	tbd	-	tbd	-	MHz
		V_{CC} = 4.5 V to 5.5 V	110	-	-	64	-	60	-	MHz

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_t	transition time	Qn and Q7S; see Fig. 12 and Fig. 13 [5]								
		V_{CC} = 2 V	-	9	13	-	15	-	16	ns
		V_{CC} = 4.5 V	-	5	7	-	8	-	8	ns
		V_{CC} = 6 V	-	4	6	-	7	-	7	ns
		V_{CC} = 3.0 V to 3.6 V	-	6	8	-	9	-	10	ns
		V_{CC} = 4.5 V to 5.5 V	-	5	7	-	8	-	8	ns
C_I	input capacitance		-	1.5	-	-	5	-	5	pF
C_{PD}	power dissipation capacitance	f_i = 1 MHz; C_L = 0 pF; V_I = GND to V_{CC}; V_{CC} = 2 V to 6 V [6][7]	-	14	-	-	-	-	-	pF

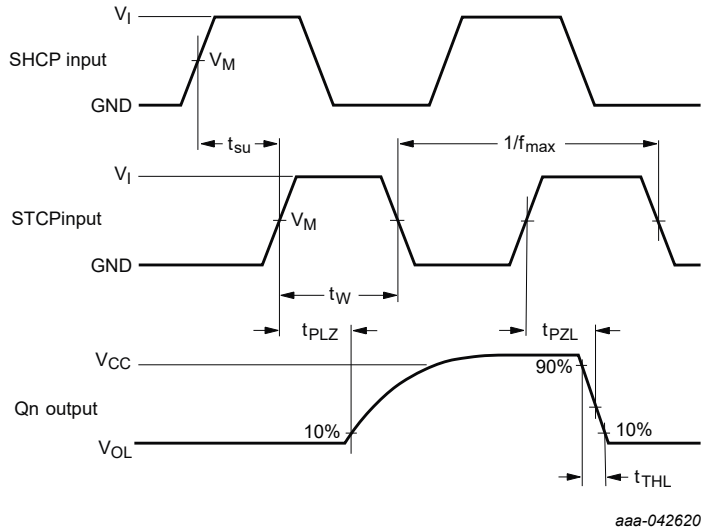
[1] Typical values are measured at nominal supply voltage.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZL}.
[4] t_{dis} is the same as t_{PLZ}.
[5] t_t is the same as t_{THL} and t_{TLH}.
[6] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.
[7] All 9 outputs switching.

11.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

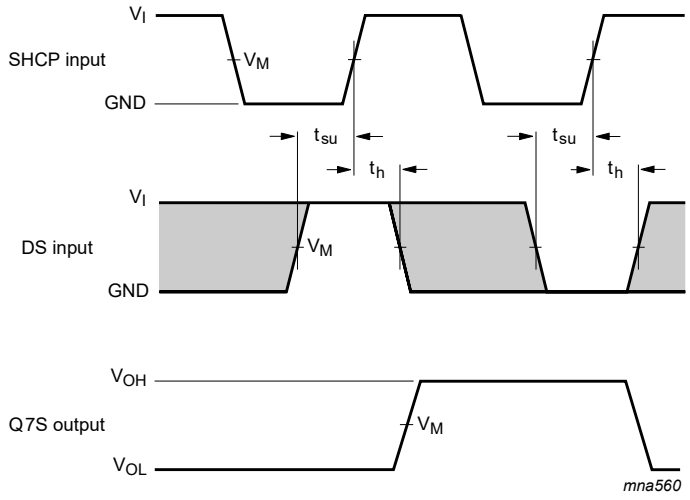
Fig. 12. Shift clock pulse, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} is the typical output voltage level that occur with the output load.

Fig. 13. Storage clock to output propagation delays

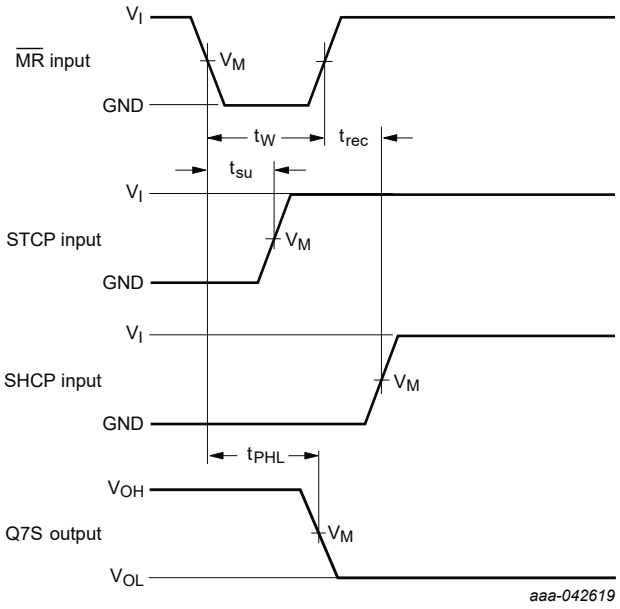


Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

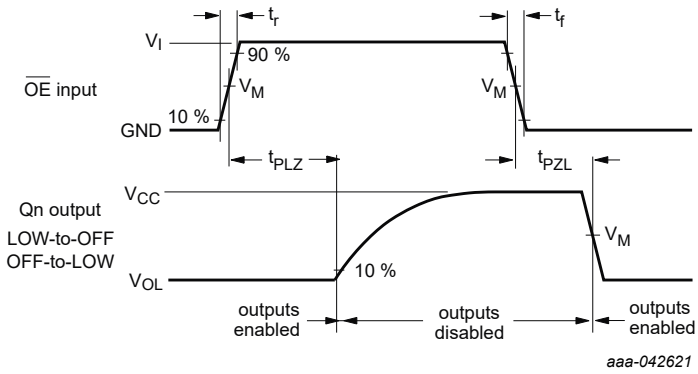
Fig. 14. Data set-up and hold times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 15. Master reset to output propagation delays



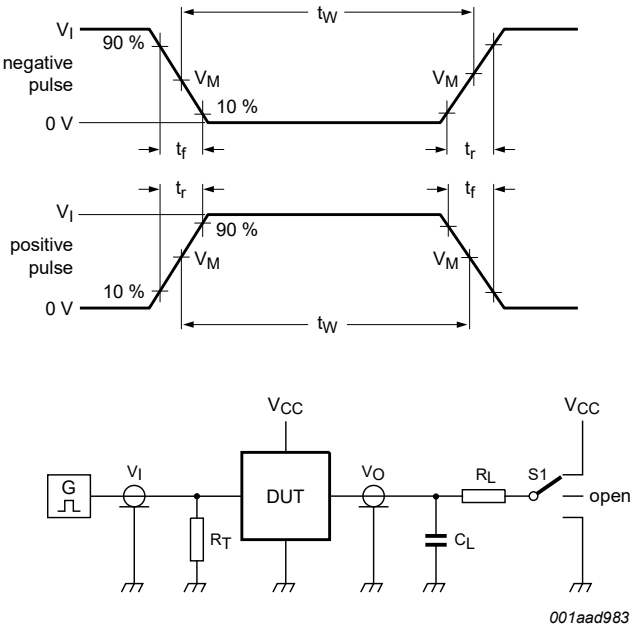
Measurement points are given in Table 8.

V_{OL} is the typical output voltage level that occur with the output load.

Fig. 16. Enable and disable times

Table 8. Measurement points

Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

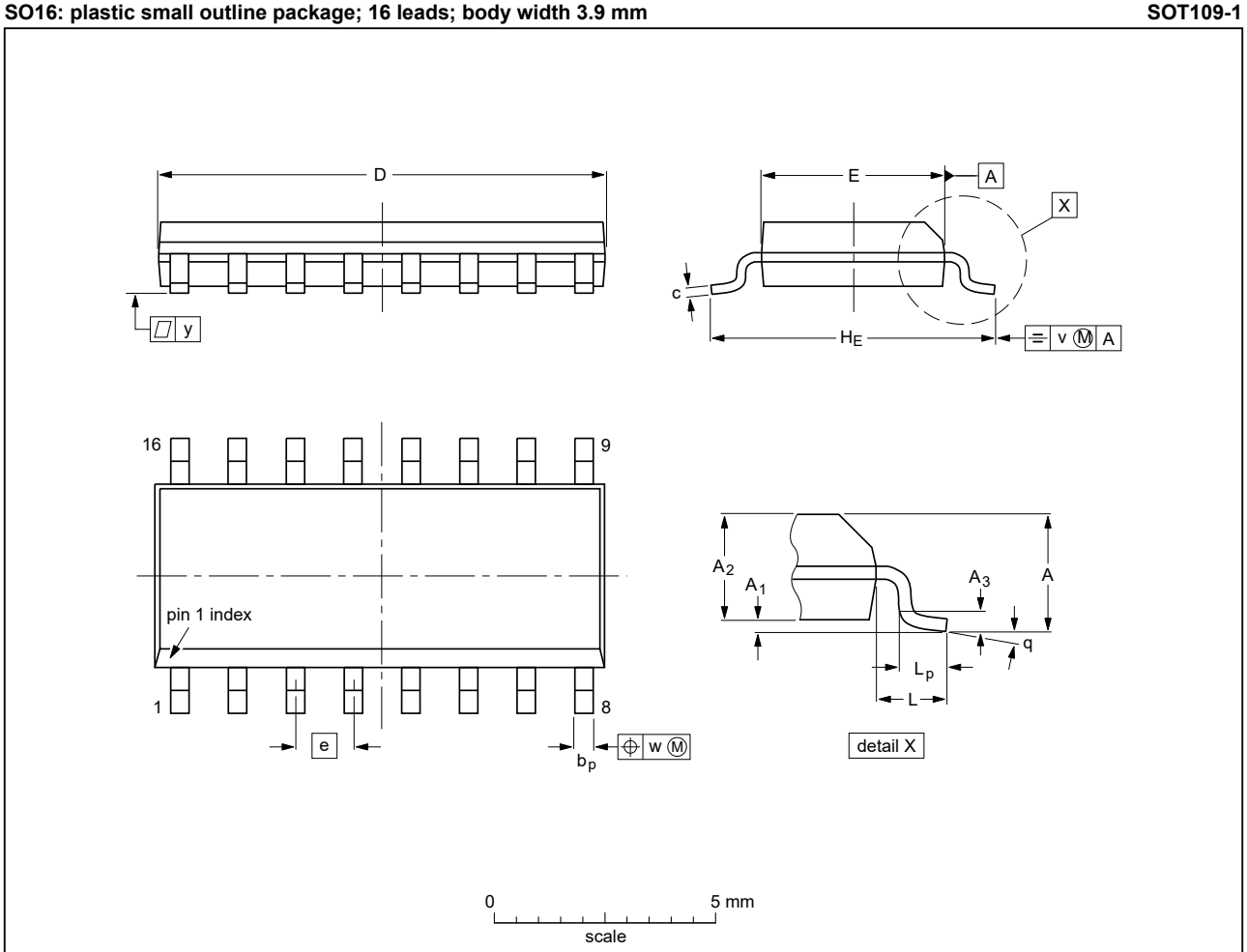
Fig. 17. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

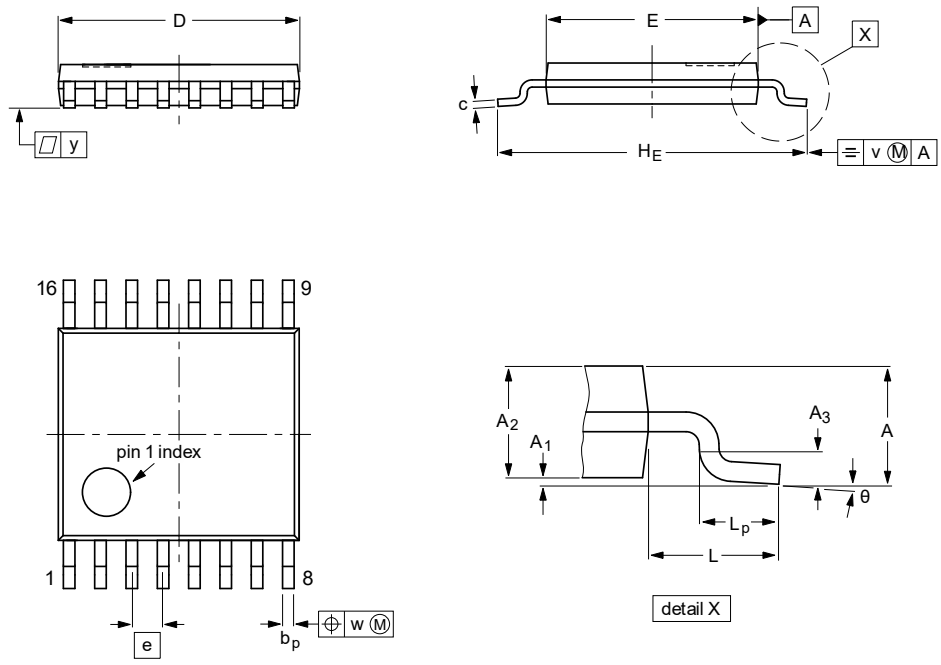
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

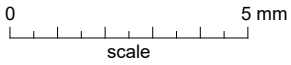
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm nom				0.25					0.65		1		0.2	0.1	0.1	
min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

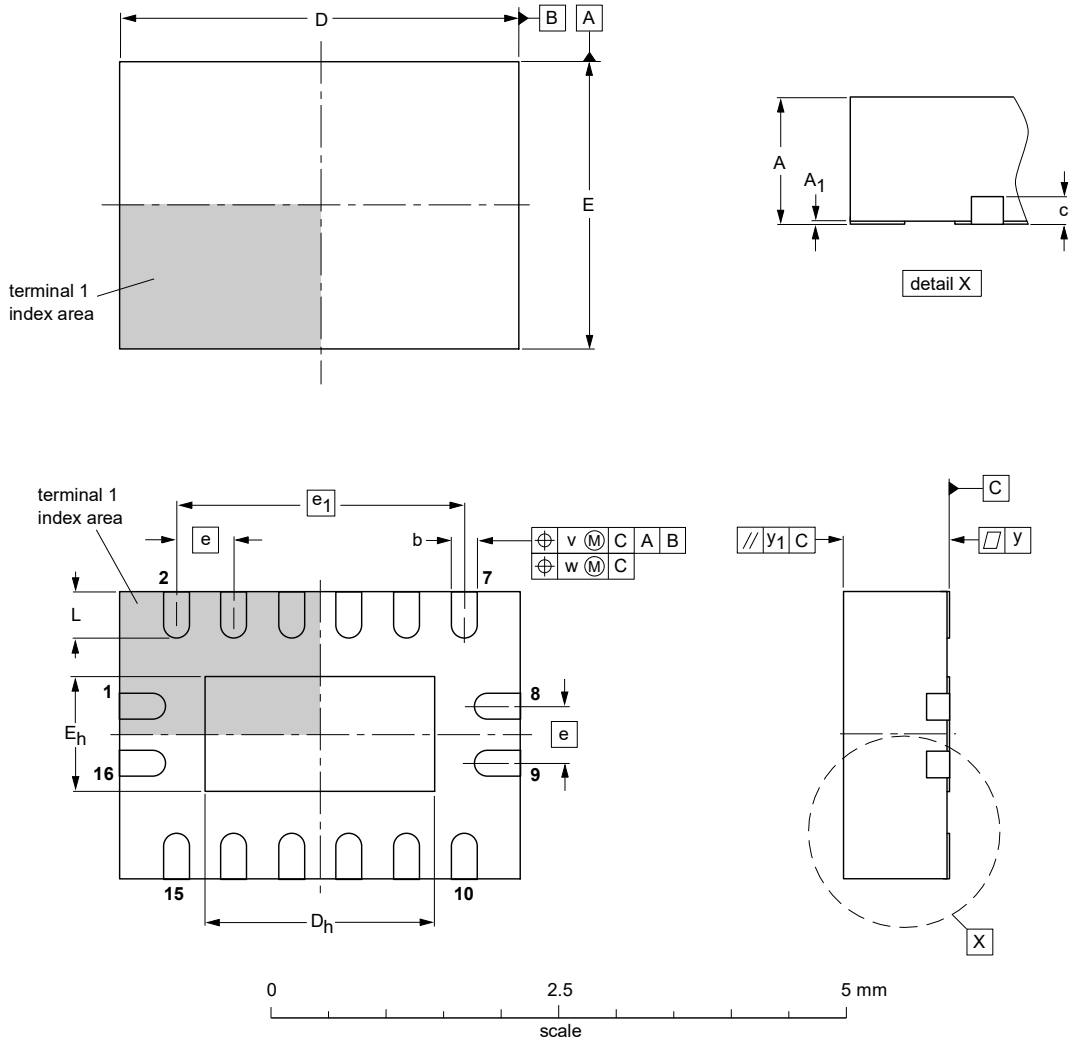
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 20. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS596 v.1	20250528	Objective data sheet	-	-

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS596_Q100 v.1.8	20250528	Objective data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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