



74HCS165

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

Rev. 1 — 23 April 2025

Product data sheet

1. General description

The 74HCS165 is an 8-bit serial or parallel-in/serial-out shift register. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input (\overline{PL}) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When \overline{PL} is HIGH data enters the register serially at DS. When the clock enable input (\overline{CE}) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on \overline{CE} will disable the CP input. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

All inputs are Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Schmitt-trigger inputs
- Low power consumption
 - Typical supply current (I_{CC}) of 100 nA
 - Typical input leakage current (I_I) of ± 10 nA
- ± 7.8 mA output drive at 6 V
- 8-bit serial input and 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 class 3A exceeds 4000 V
 - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Applications

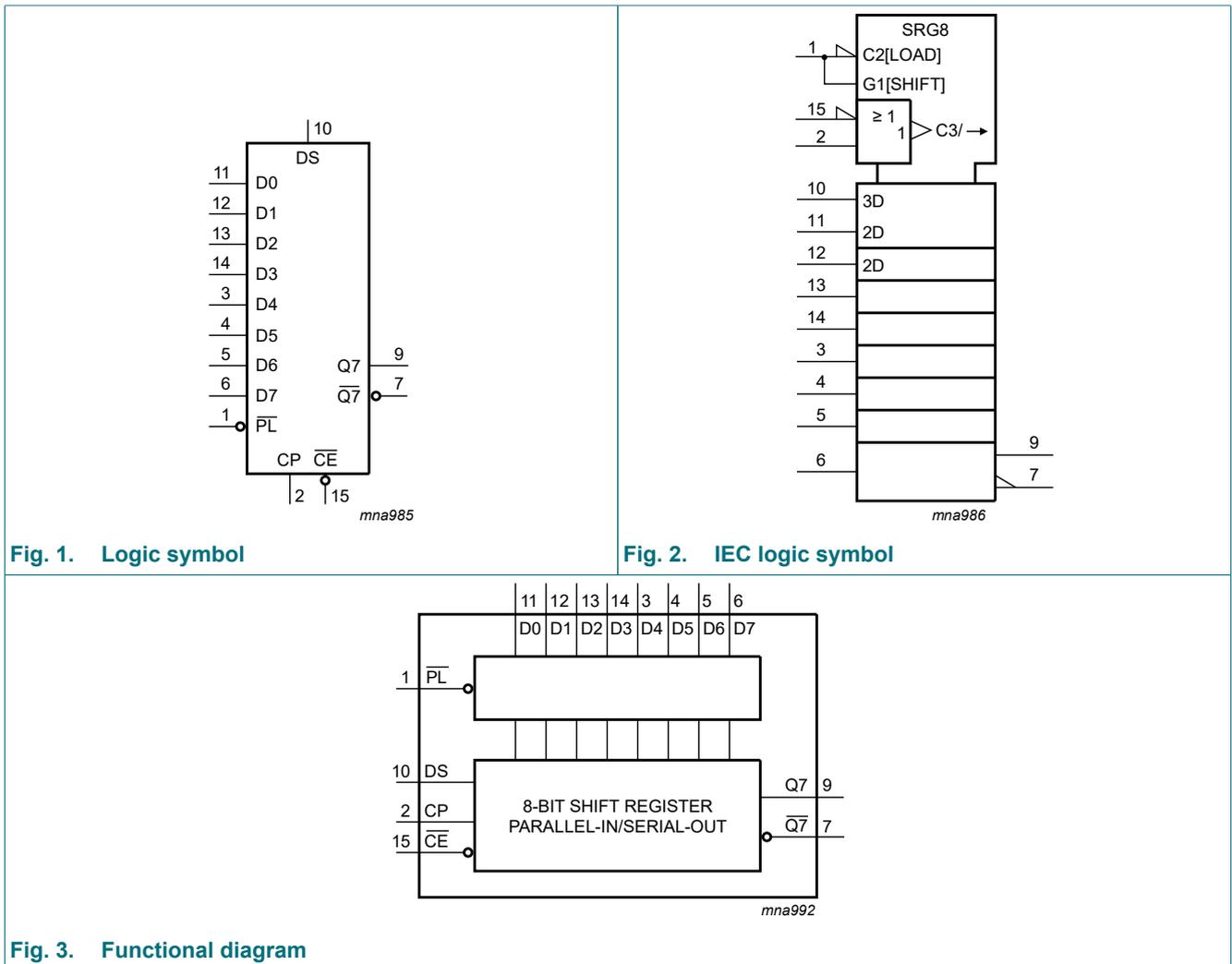
- Parallel-to-serial data conversion
- Remote control holding register
- Output expansion
- LED matrix control
- 7-segment display control
- 8-bit data storage

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HCS165D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCS165PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCS165BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram



8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

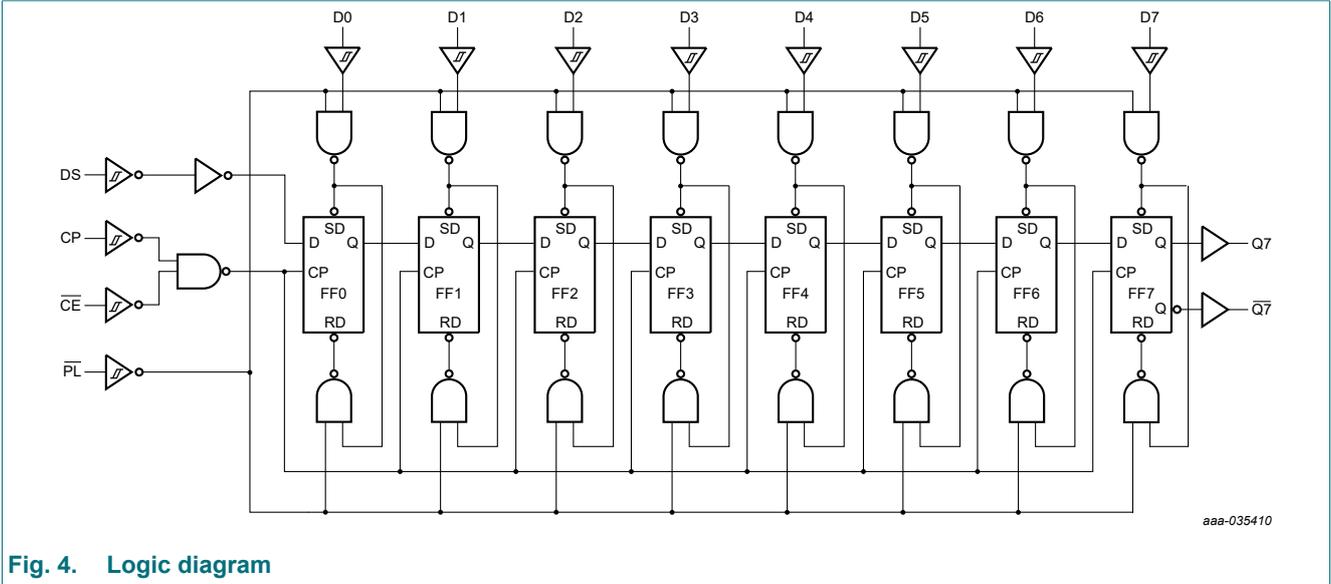
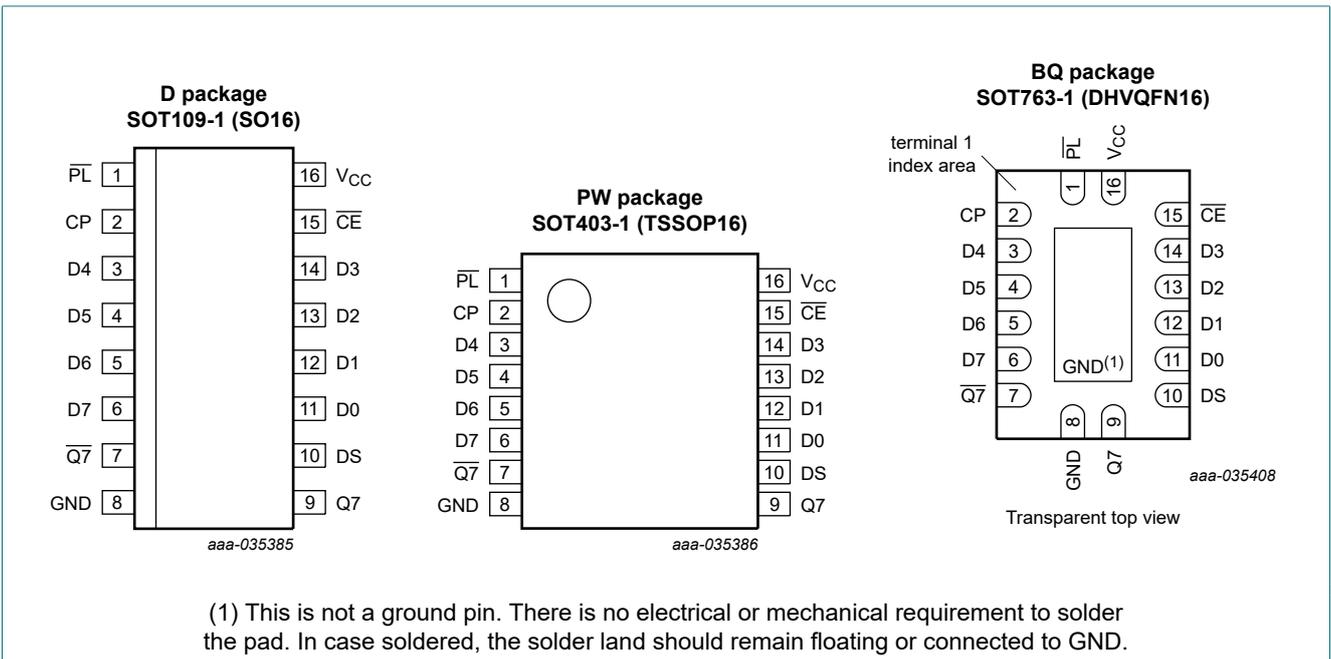


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
PL	1	asynchronous parallel load input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
$\overline{Q7}$	7	complementary output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs (also referred to as Dn)
\overline{CE}	15	clock enable input (active LOW)
V _{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs					Qn registers		Outputs	
	PL	\overline{CE}	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

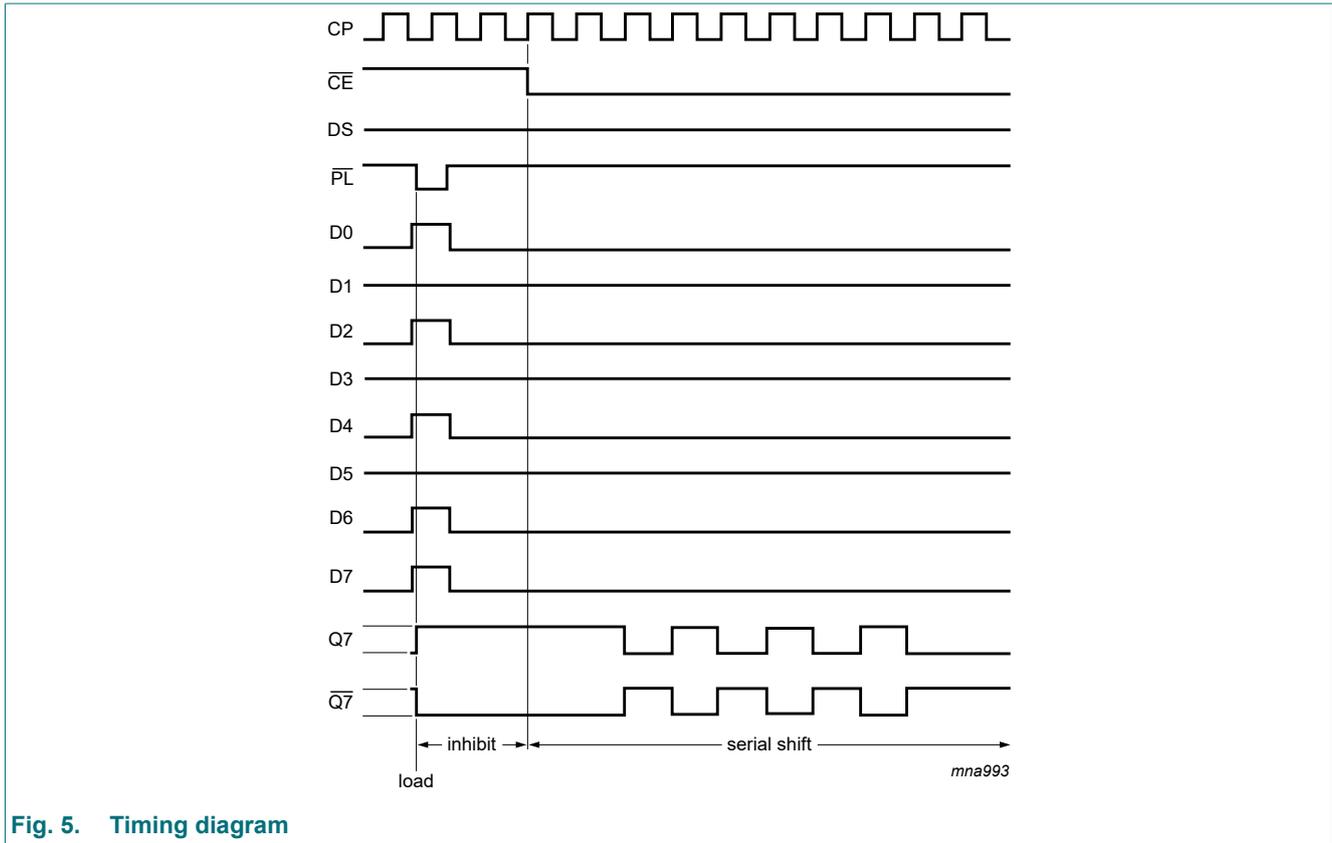


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = 0\text{ V}$ to V_{CC}	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_j	junction temperature	[2]	-	+150	°C
T_{stg}	storage temperature		-65	+150	°C
V_{ESD}	electrostatic discharge	HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4000 V	-	± 4000	V
		CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1500 V	-	± 1500	V
P_{tot}	total power dissipation	[3]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Guaranteed by design.

[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 6 and Fig. 7								
		$V_{CC} = 2.0\text{ V}$	0.7	-	1.5	0.7	1.5	0.7	1.5	V
		$V_{CC} = 4.5\text{ V}$	1.7	-	3.15	1.7	3.15	1.7	3.15	V
		$V_{CC} = 6\text{ V}$	2.1	-	4.2	2.1	4.2	2.1	4.2	V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	$0.4V_{CC}$	-	$0.7V_{CC}$	$0.4V_{CC}$	$0.7V_{CC}$	$0.4V_{CC}$	$0.7V_{CC}$	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.38V_{CC}$	-	$0.7V_{CC}$	$0.38V_{CC}$	$0.7V_{CC}$	$0.38V_{CC}$	$0.7V_{CC}$	V
V_{T-}	negative-going threshold voltage	see Fig. 6 and Fig. 7								
		$V_{CC} = 2.0\text{ V}$	0.3	-	1.0	0.3	1.0	0.3	1.0	V
		$V_{CC} = 4.5\text{ V}$	0.9	-	2.2	0.9	2.2	0.9	2.2	V
		$V_{CC} = 6\text{ V}$	1.2	-	3.0	1.2	3.0	1.2	3.0	V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	$0.2V_{CC}$	-	$0.5V_{CC}$	$0.2V_{CC}$	$0.5V_{CC}$	$0.2V_{CC}$	$0.5V_{CC}$	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.2V_{CC}$	-	$0.49V_{CC}$	$0.2V_{CC}$	$0.49V_{CC}$	$0.2V_{CC}$	$0.49V_{CC}$	V
V_H	hysteresis voltage[1]	see Fig. 6 and Fig. 7								
		$V_{CC} = 2.0\text{ V}$	0.2	0.52	1.0	0.2	1.0	0.2	1.0	V
		$V_{CC} = 4.5\text{ V}$	0.4	0.85	1.4	0.4	1.4	0.4	1.4	V
		$V_{CC} = 6\text{ V}$	0.6	1.1	1.6	0.6	1.6	0.6	1.6	V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	$0.1V_{CC}$	0.72	$0.38V_{CC}$	$0.1V_{CC}$	$0.38V_{CC}$	$0.1V_{CC}$	$0.38V_{CC}$	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.09V_{CC}$	0.94	$0.29V_{CC}$	$0.09V_{CC}$	$0.29V_{CC}$	$0.09V_{CC}$	$0.29V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_{OH} = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V to }6\text{ V}$	$V_{CC}-0.1$	$V_{CC}-0.002$	-	$V_{CC}-0.1$	-	$V_{CC}-0.1$	-	V
		$I_{OH} = -4\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.7	2.85	-	2.7	-	2.7	-	V
		$I_{OH} = -6\text{ mA}$; $V_{CC} = 4.5\text{ V}$	4.0	4.3	-	4.0	-	4.0	-	V
		$I_{OH} = -7.8\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.48	5.75	-	5.4	-	5.4	-	V

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _{OL} = 20 μA; V _{CC} = 2.0 V to 6 V	-	0.002	0.1	-	0.1	-	0.1	V
		I _{OH} = 4 mA; V _{CC} = 3.0 V	-	0.14	0.25	-	0.25	-	0.25	V
		I _{OL} = 6 mA; V _{CC} = 4.5 V	-	0.18	0.26	-	0.30	-	0.30	V
		I _{OL} = 7.8 mA; V _{CC} = 6.0 V	-	0.22	0.26	-	0.33	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	±0.01	±0.1	-	±0.25	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	0.1	-	-	0.5	-	2.0	μA

[1] Guaranteed by design.

10.1. Transfer characteristic waveforms and graphs

10.1.1. For inputs

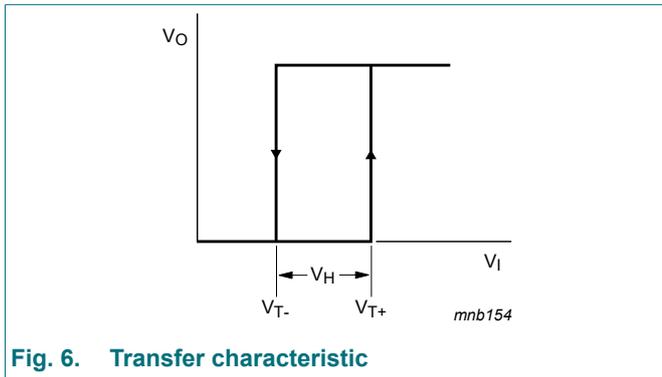


Fig. 6. Transfer characteristic

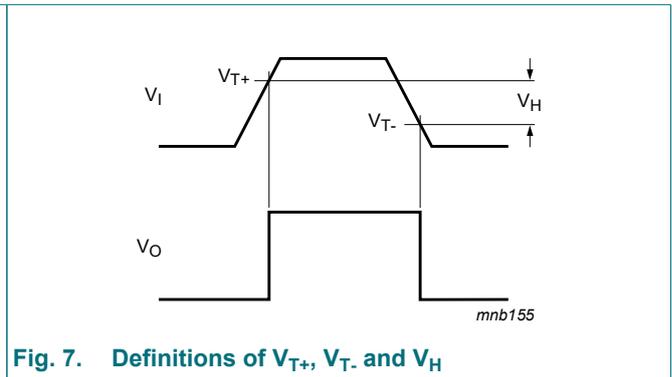


Fig. 7. Definitions of V_{T+}, V_{T-} and V_H

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

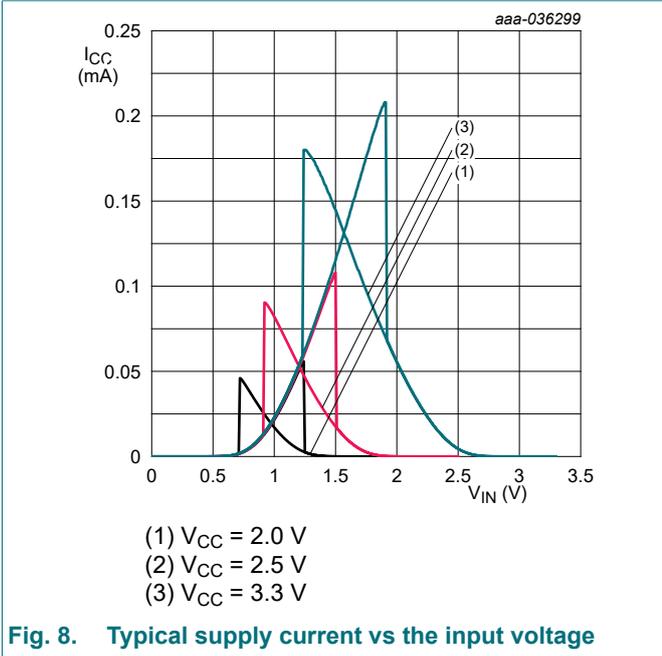


Fig. 8. Typical supply current vs the input voltage

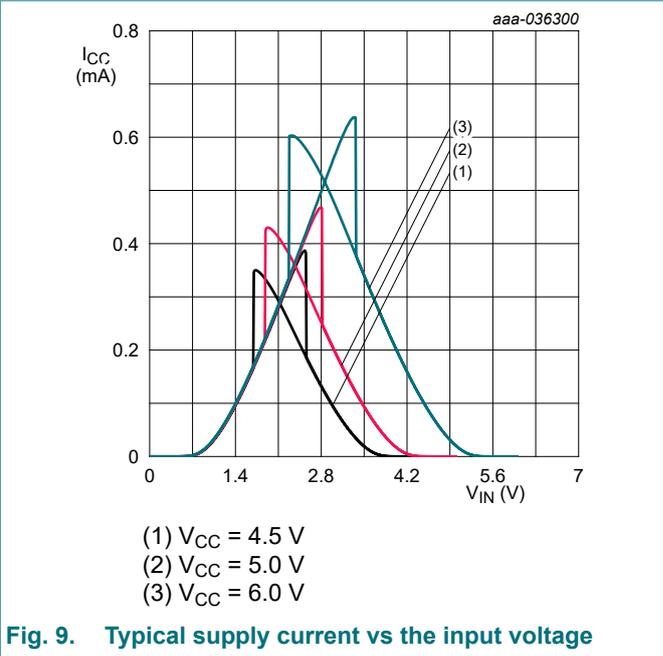


Fig. 9. Typical supply current vs the input voltage

10.1.2. For outputs

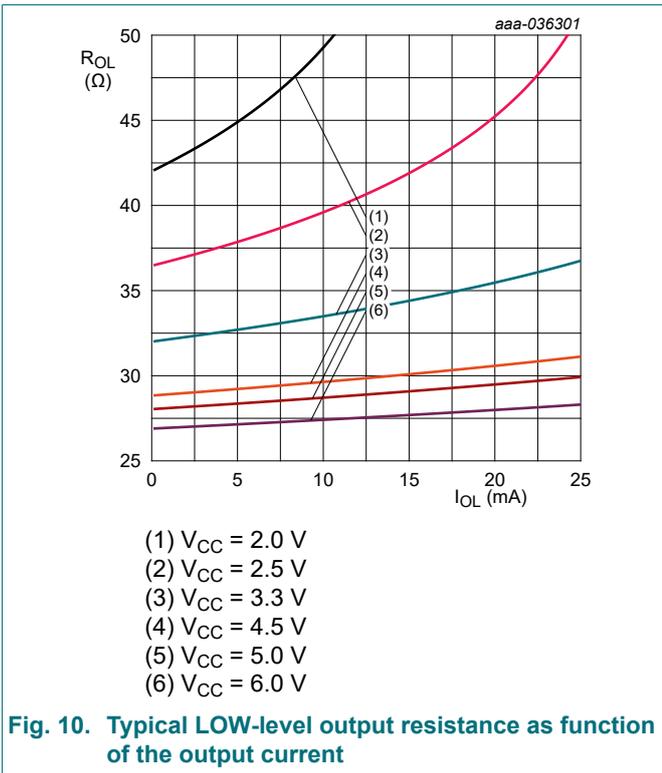


Fig. 10. Typical LOW-level output resistance as function of the output current

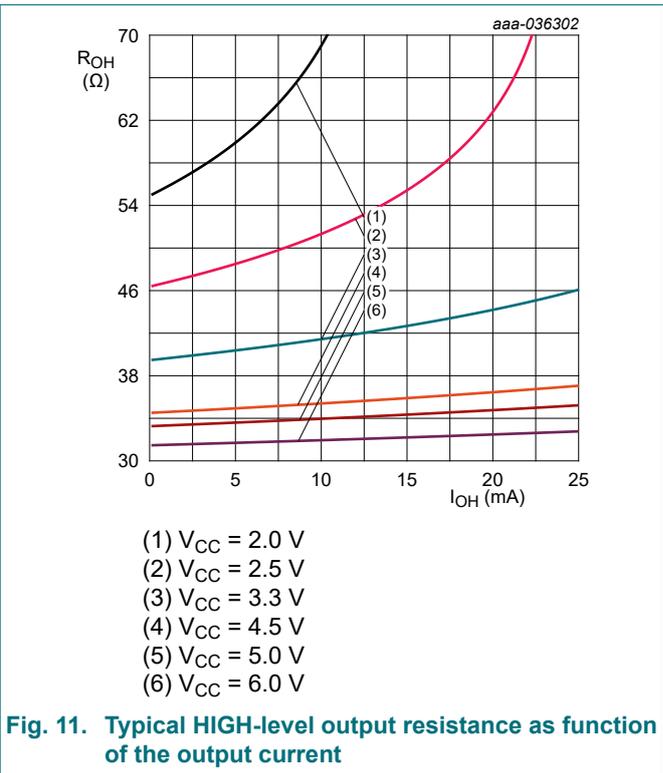


Fig. 11. Typical HIGH-level output resistance as function of the output current

11. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 17.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to Q7, $\overline{Q7}$; see Fig. 12 [2]								
		$V_{CC} = 2.0\text{ V}$	-	16	32	-	42	-	45	ns
		$V_{CC} = 4.5\text{ V}$	-	8	16	-	17	-	18	ns
		$V_{CC} = 6.0\text{ V}$	-	7	14	-	15	-	16	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	10	20	-	21	-	23	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	8	16	-	17	-	18	ns
		\overline{PL} to Q7, $\overline{Q7}$; see Fig. 13								
		$V_{CC} = 2.0\text{ V}$	-	20	39	-	60	-	65	ns
		$V_{CC} = 4.5\text{ V}$	-	10	19	-	22	-	24	ns
		$V_{CC} = 6.0\text{ V}$	-	8	17	-	18	-	19	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	12	25	-	28	-	31	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	9	19	-	22	-	24	ns
		D7 to Q7, $\overline{Q7}$; see Fig. 14								
		$V_{CC} = 2.0\text{ V}$	-	20	30	-	44	-	48	ns
		$V_{CC} = 4.5\text{ V}$	-	9	15	-	17	-	18	ns
$V_{CC} = 6.0\text{ V}$	-	8	14	-	15	-	16	ns		
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	12	20	-	22	-	24	ns		
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	9	15	-	17	-	18	ns		
t_t	transition time	Q7, $\overline{Q7}$ output; see Fig. 12 [3]								
		$V_{CC} = 2.0\text{ V}$	-	9	13	-	15	-	16	ns
		$V_{CC} = 4.5\text{ V}$	-	5	7	-	8	-	8	ns
		$V_{CC} = 6.0\text{ V}$	-	4	6	-	7	-	7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	5	8	-	9	-	10	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	4	7	-	8	-	8	ns
t_w	pulse width	CP input HIGH or LOW; see Fig. 12								
		$V_{CC} = 2.0\text{ V}$	7	-	-	10	-	11	-	ns
		$V_{CC} = 4.5\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 6.0\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	7	-	-	8	-	9	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	6	-	-	7	-	7	-	ns
		\overline{PL} input LOW; see Fig. 13								
		$V_{CC} = 2.0\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 4.5\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 6.0\text{ V}$	6	-	-	7	-	7	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	6	-	-	7	-	7	-	ns
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	6	-	-	7	-	7	-	ns		

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

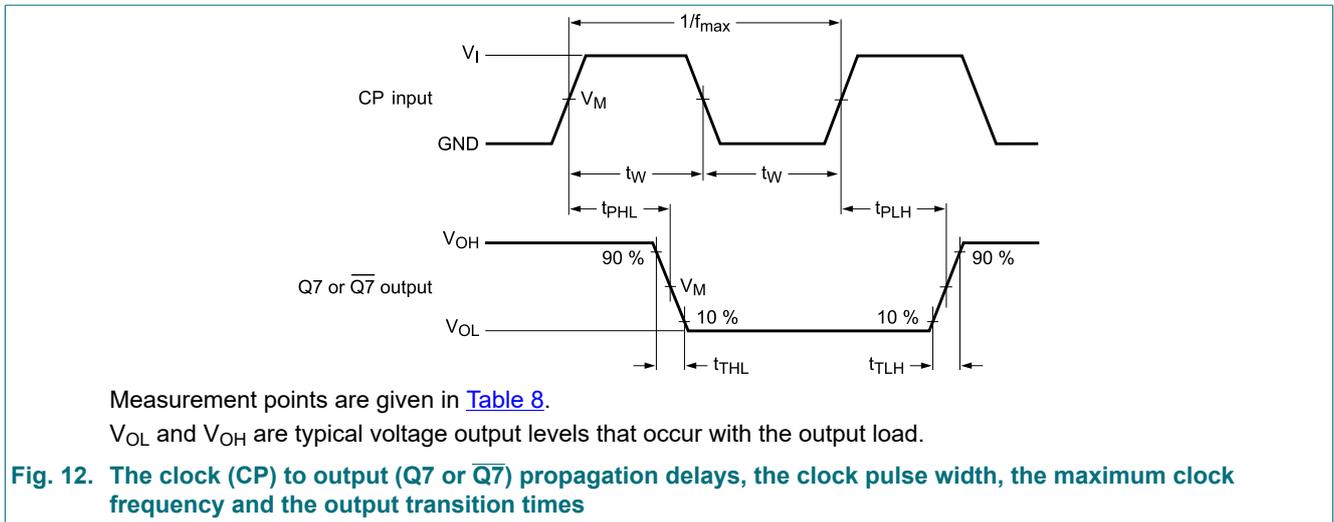
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{rec}	recovery time	\overline{PL} input HIGH to CP; see Fig. 13								
		V _{CC} = 2.0 V	13	-	-	19	-	21	-	ns
		V _{CC} = 4.5 V	5	-	-	7	-	7	-	ns
		V _{CC} = 6.0 V	4	-	-	6	-	6	-	ns
		V _{CC} = 3.0 V to 3.6 V	6	-	-	8	-	8	-	ns
		V _{CC} = 4.5 V to 5.5 V	5	-	-	7	-	7	-	ns
t _{su}	set-up time	DS to CP; see Fig. 15								
		V _{CC} = 2.0 V	8	-	-	13	-	14	-	ns
		V _{CC} = 4.5 V	4	-	-	6	-	6	-	ns
		V _{CC} = 6.0 V	4	-	-	6	-	6	-	ns
		V _{CC} = 3.0 V to 3.6 V	6	-	-	9	-	10	-	ns
		V _{CC} = 4.5 V to 5.5 V	4	-	-	6	-	6	-	ns
		\overline{CE} HIGH or LOW to CP; see Fig. 15								
		V _{CC} = 2.0 V	6	-	-	9	-	9	-	ns
		V _{CC} = 4.5 V	4	-	-	5	-	5	-	ns
		V _{CC} = 6.0 V	4	-	-	5	-	5	-	ns
		V _{CC} = 3.0 V to 3.6 V	6	-	-	7	-	7	-	ns
		V _{CC} = 4.5 V to 5.5 V	4	-	-	5	-	5	-	ns
		Dn to \overline{PL} ; see Fig. 16								
		V _{CC} = 2.0 V	9	-	-	17	-	17	-	ns
		V _{CC} = 4.5 V	4	-	-	6	-	6	-	ns
		V _{CC} = 6.0 V	4	-	-	6	-	6	-	ns
		V _{CC} = 3.0 V to 3.6 V	7	-	-	10	-	10	-	ns
		V _{CC} = 4.5 V to 5.5 V	4	-	-	6	-	6	-	ns
t _h	hold time	DS to CP; see Fig. 15								
		V _{CC} = 2.0 V	0	-	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-	-	0	-	0	-	ns
		V _{CC} = 6.0 V	0	-	-	0	-	0	-	ns
		V _{CC} = 3.0 V to 3.6 V	0	-	-	0	-	0	-	ns
		V _{CC} = 4.5 V to 5.5 V	0	-	-	0	-	0	-	ns
		Dn to \overline{PL} ; see Fig. 16								
		V _{CC} = 2.0 V	5	-	-	6	-	6	-	ns
		V _{CC} = 4.5 V	4	-	-	5	-	5	-	ns
		V _{CC} = 6.0 V	3	-	-	4	-	4	-	ns
		V _{CC} = 3.0 V to 3.6 V	5	-	-	6	-	6	-	ns
		V _{CC} = 4.5 V to 5.5 V	4	-	-	5	-	5	-	ns

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

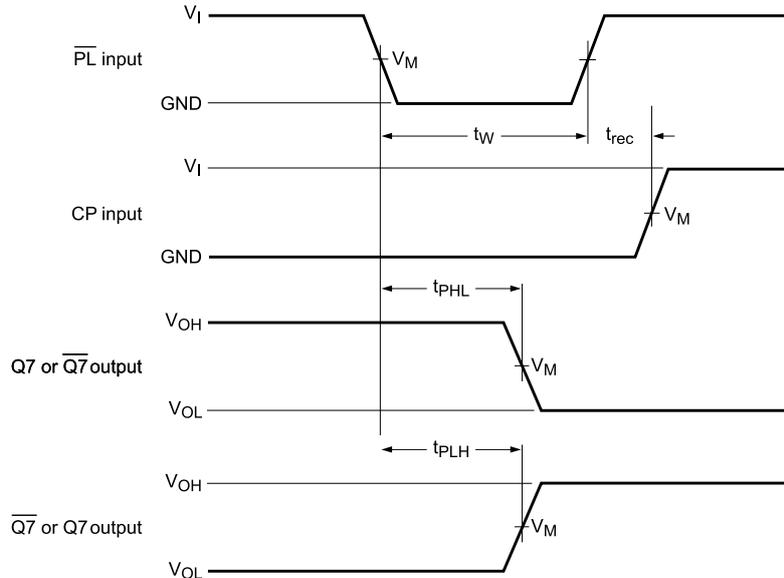
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	CP input; see Fig. 12								
		V _{CC} = 2.0 V	49	-	-	47	-	43	-	MHz
		V _{CC} = 4.5 V	130	-	-	122	-	120	-	MHz
		V _{CC} = 6.0 V	170	-	-	155	-	150	-	MHz
		V _{CC} = 3.0 V to 3.6 V	109	-	-	105	-	96	-	MHz
		V _{CC} = 4.5 V to 5.5 V	130	-	-	122	-	120	-	MHz
C _I	input capacitance		-	1.5	-	-	5	-	5	pF
C _{PD}	power dissipation capacitance	f _i = 1 MHz; C _L = 0 pF; V _I = GND to V _{CC} ; V _{CC} = 2 V to 6 V	[4][5]	-	20	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage.
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [3] t_t is the same as t_{THL} and t_{TLH}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.
- [5] All 9 inputs switching.

11.1. Waveforms and test circuit



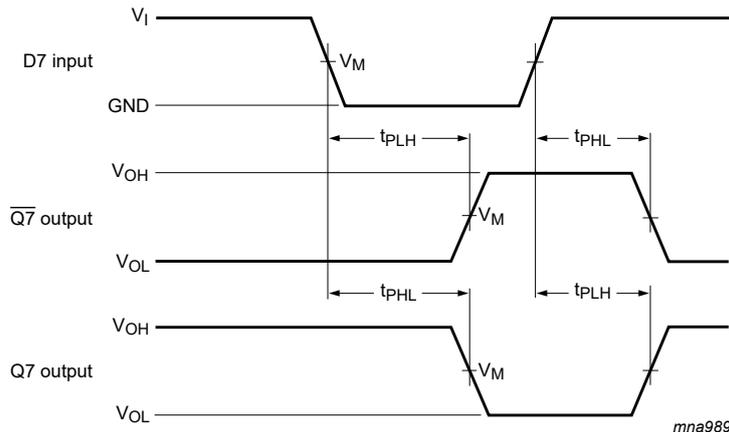
8-bit parallel-in/serial out shift register with Schmitt-trigger inputs



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 13. The parallel load (\overline{PL}) pulse width, the parallel load to output ($Q7$ or $\overline{Q7}$) propagation delays, the parallel load to clock (CP) recovery times

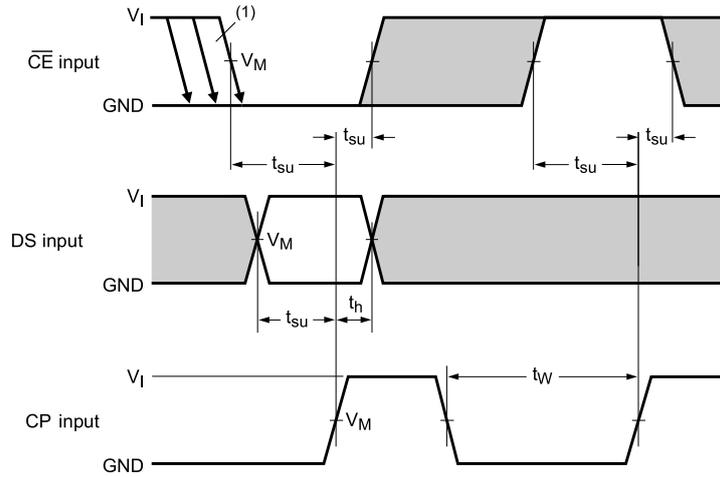


Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

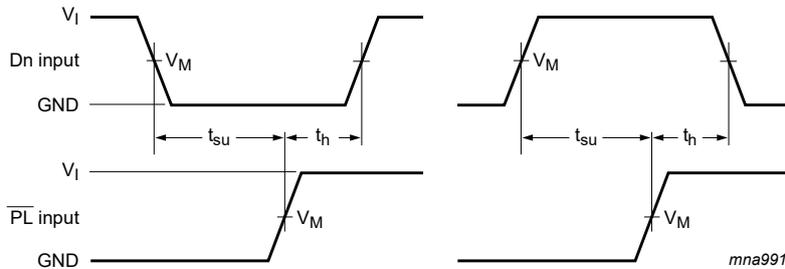
Fig. 14. The data input ($D7$) to output ($Q7$ or $\overline{Q7}$) propagation delays when \overline{PL} is LOW

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs



(1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW.
 The shaded areas indicate when the input is permitted to change for predictable output performance
 Measurement points are given in [Table 8](#).

Fig. 15. The set-up and hold times from the serial data input (DS) to the clock input (CP) and from the clock enable input (\overline{CE}) to the clock input (CP)



Measurement points are given in [Table 8](#).

Fig. 16. The set-up and hold times from the data inputs (Dn) to the parallel load input (\overline{PL})

Table 8. Measurement points

Input	Output
V_M	V_M
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

8-bit parallel-in/serial out shift register with Schmitt-trigger inputs

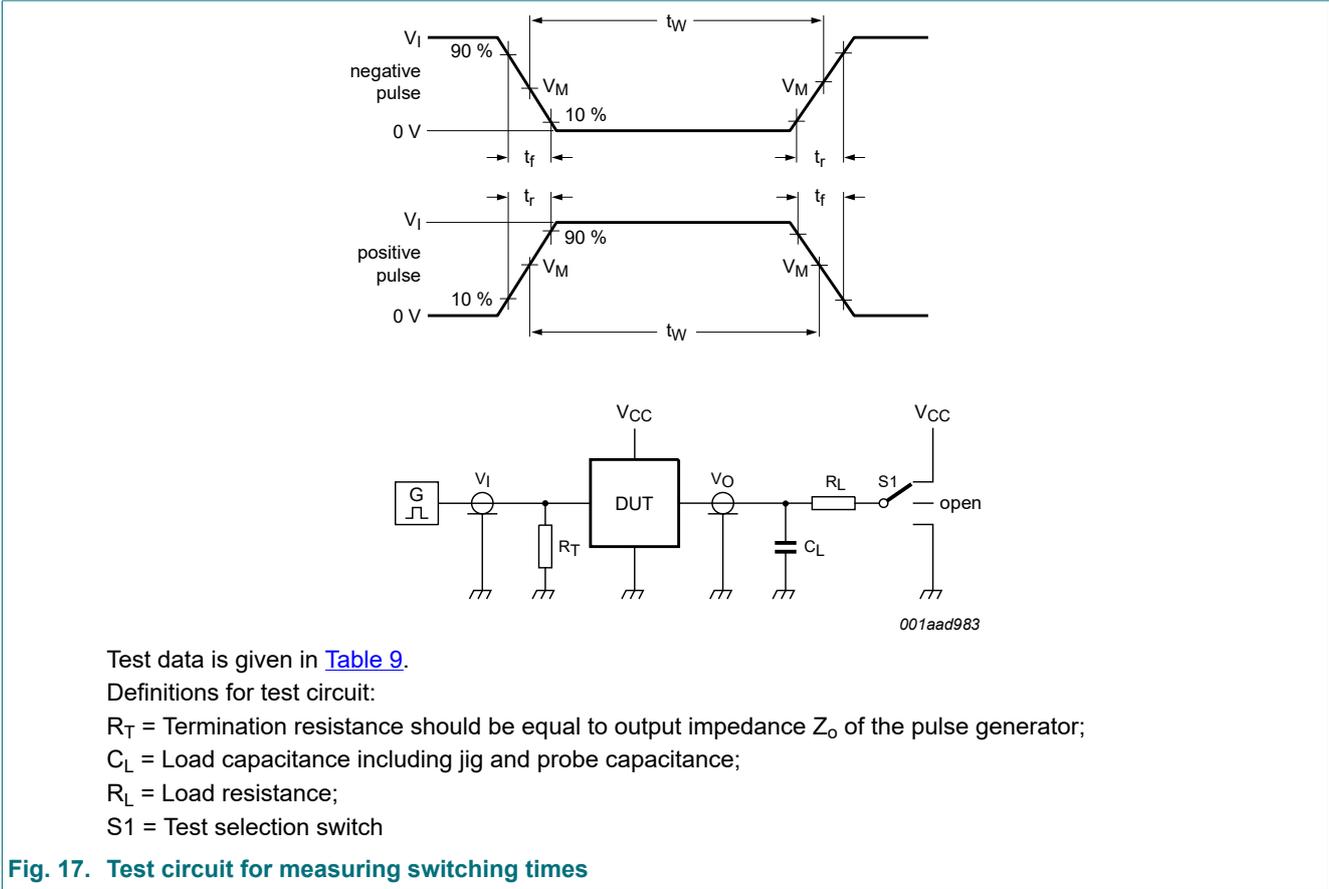


Fig. 17. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	2.5 ns	50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

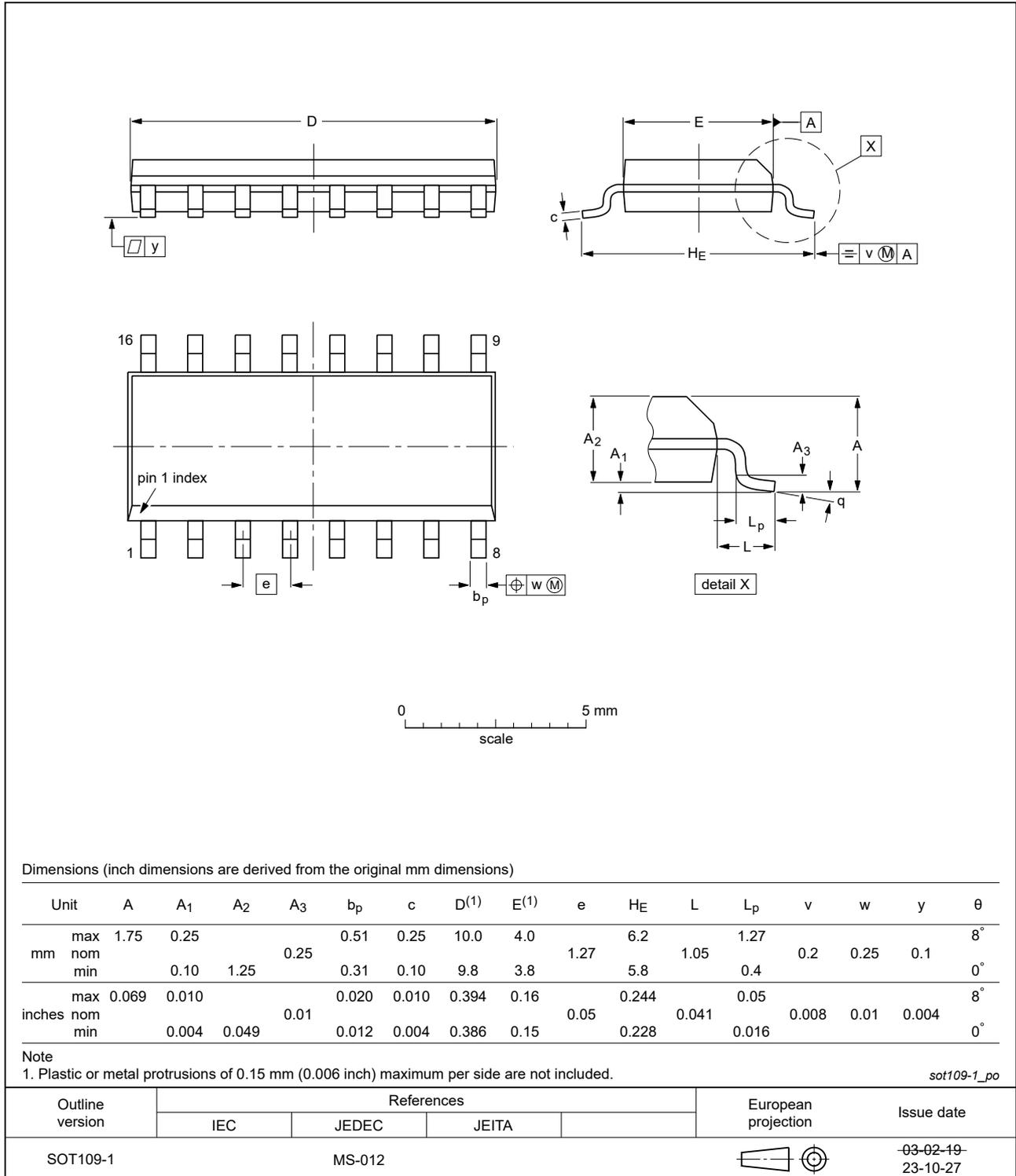


Fig. 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

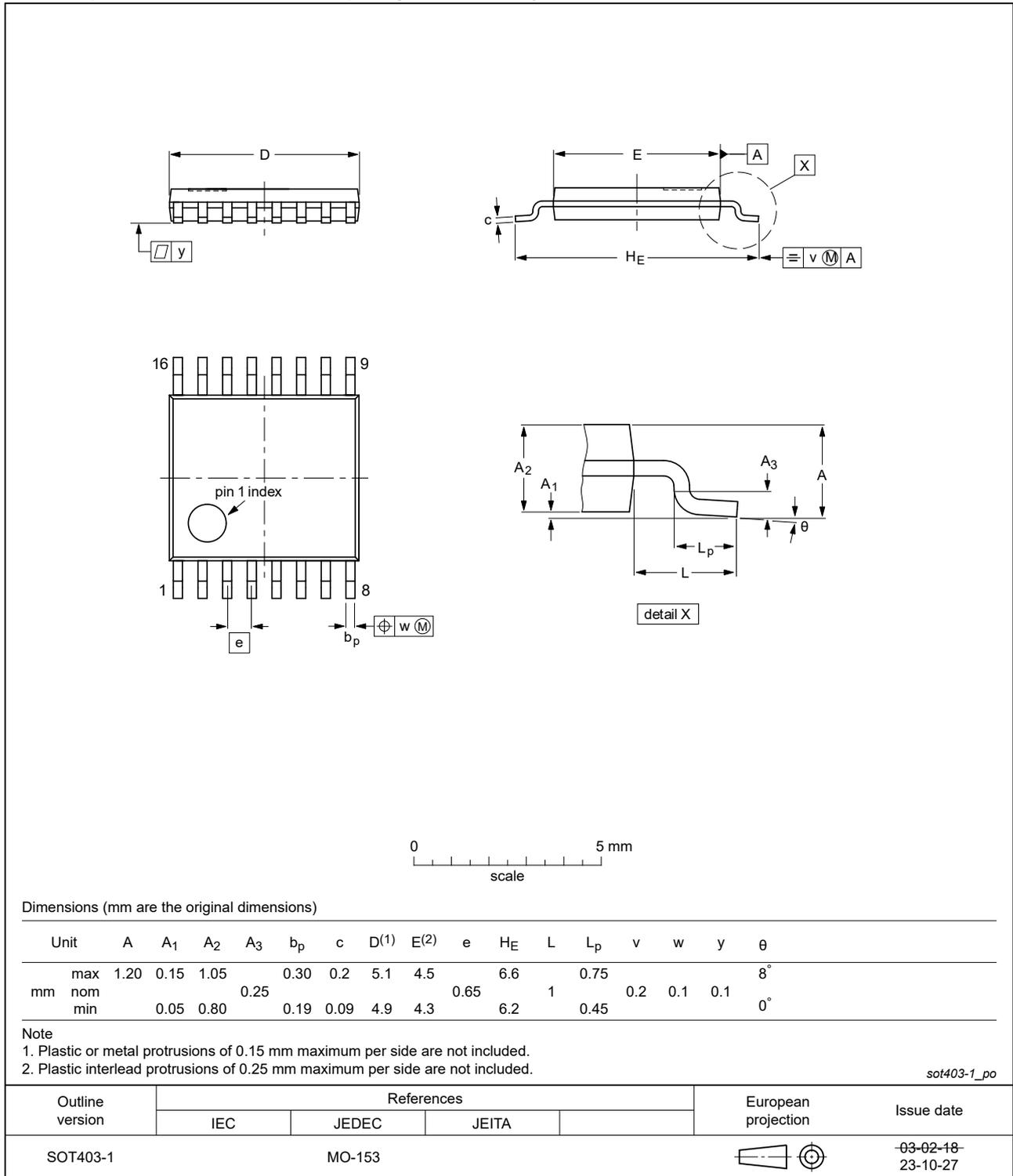


Fig. 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

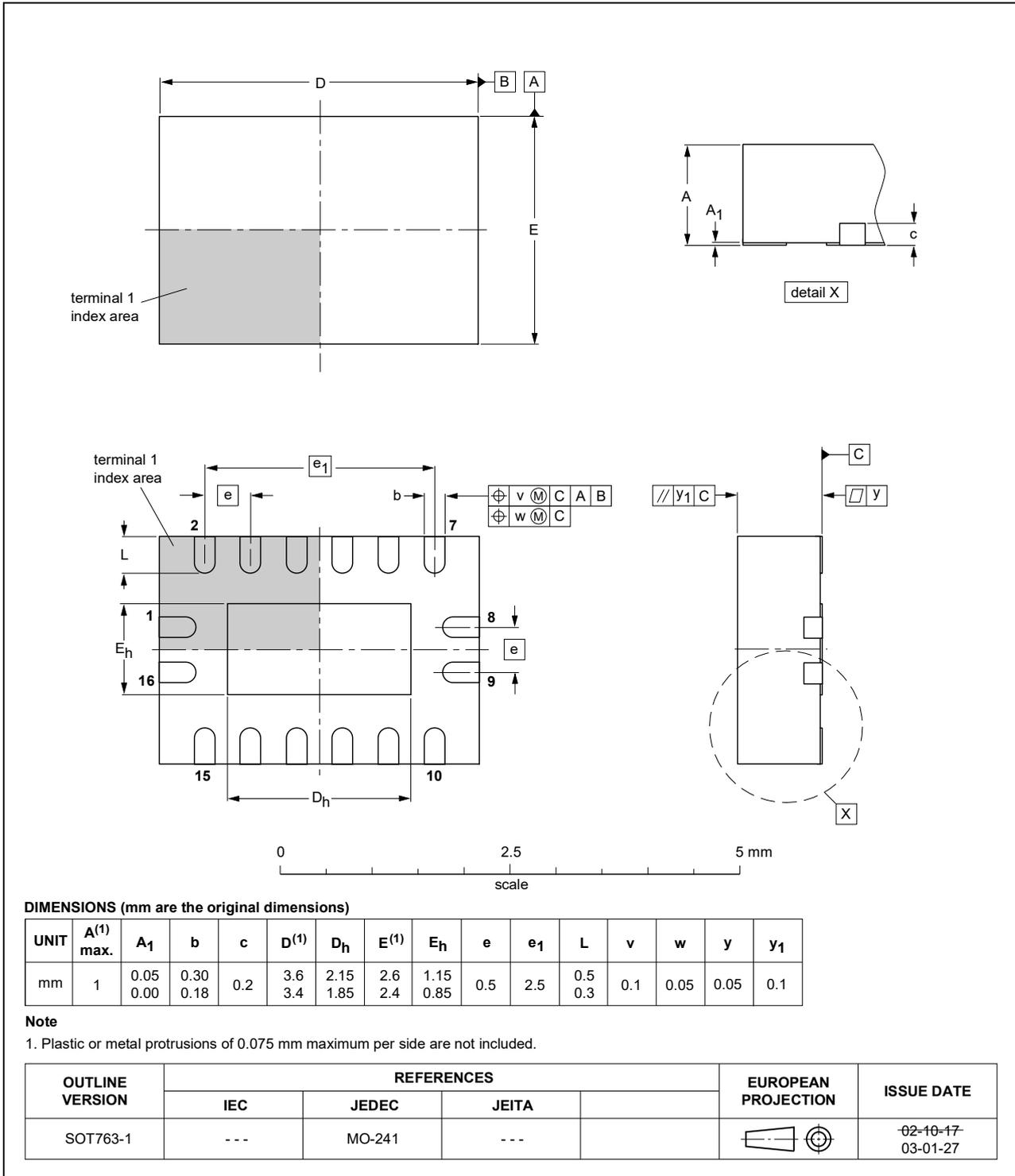


Fig. 20. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS165 v.1	20250527	Product data sheet	-	-

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCS165_Q100 v.1	20250527	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description	1
2. Features and benefits	1
3. Applications	1
4. Ordering information	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	4
7. Functional description	4
8. Limiting values	5
9. Recommended operating conditions	6
10. Static characteristics	6
10.1. Transfer characteristic waveforms and graphs.....	7
10.1.1. For inputs.....	7
10.1.2. For outputs.....	8
11. Dynamic characteristics	9
11.1. Waveforms and test circuit.....	11
12. Package outline	15
13. Abbreviations	18
14. Revision history	18
15. Legal information	19

© Nexperia B.V. 2025. All rights reserved

For more information, please visit: <http://www.nexperia.com>
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 23 April 2025
